

Model Name : Z5W1M  
File Name : LA-B511P

# Compal Confidential

## EA52\_BM UMA M/B Schematics Document

Intel Bay Trail M

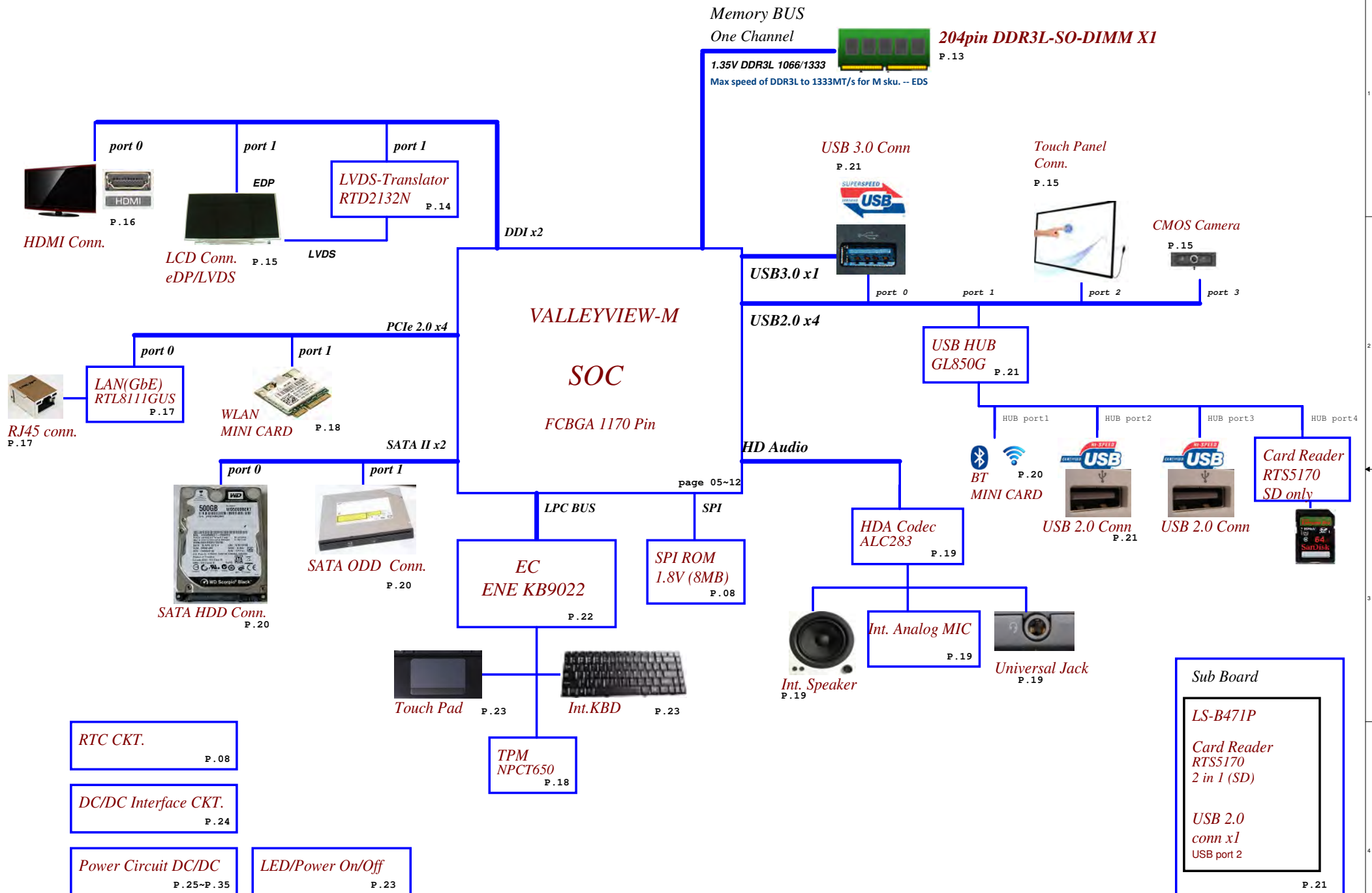
2014-03-13

REV: 1.0

PCB@  
DAX\_PCB 12R LA-B211P REV0 M/B

Part Number	Description
DA600161000	PCB 12R LA-B511P REV0 M/B

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				Customer		
				Date: Thursday, March 13, 2014	Sheet 1 of 39	



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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Block Diagrams	
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				Bay Trail M LA-B511P	1.0
				Date: Thursday, March 13, 2014	Sheet 2 of 39

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	12K +/- 5%	0.347 V	0.354 V	0.360 V
2	15K +/- 5%	0.423 V	0.430 V	0.438 V
3	20K +/- 5%	0.541 V	0.550 V	0.559 V
4	27K +/- 5%	0.691 V	0.702 V	0.713 V
5	33K +/- 5%	0.807 V	0.819 V	0.831 V
6	43K +/- 5%	0.978 V	0.992 V	1.006 V
7	56K +/- 5%	1.169 V	1.185 V	1.200 V
8	75K +/- 5%	1.398 V	1.414 V	1.430 V
9	100K +/- 5%	1.634 V	1.650 V	1.667 V
10	130K +/- 5%	1.849 V	1.865 V	1.881 V
11	160K +/- 5%	2.015 V	2.031 V	2.046 V
12	200K +/- 5%	2.185 V	2.200 V	2.215 V
13	240K +/- 5%	2.316 V	2.329 V	2.343 V

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	DVT
2	PVT
3	Pre-MP & MP
4	
5	
6	

43 level BOM table

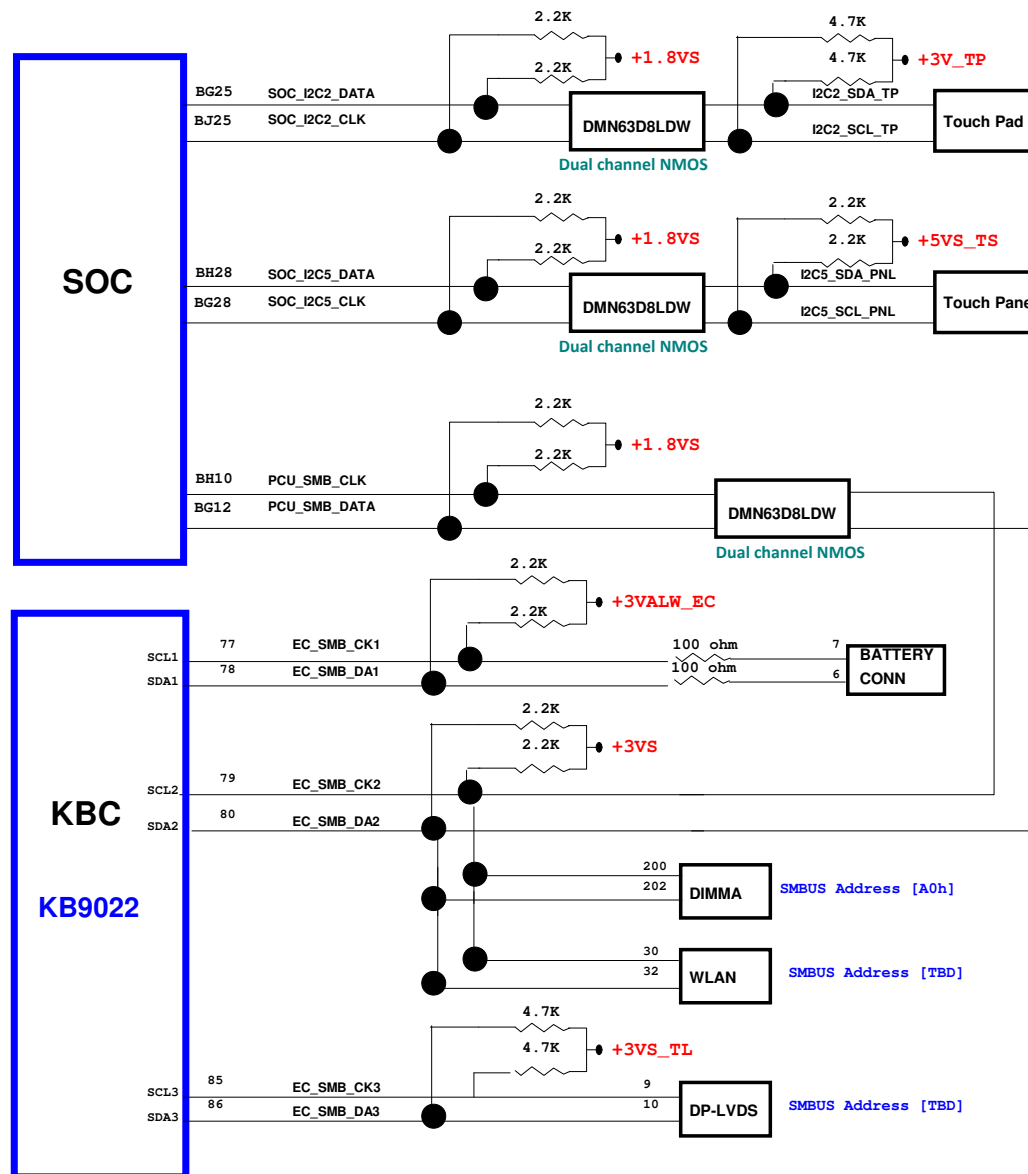
43 Level	Description	BOM Structure
4319TDBOL01	SMT MB AB511 Z5W1M UMA 2.17G	N3520@/EMC@/AMIC@/EDP@/DBG@/TPM@/PCB@/TS@
4319TDBOL02	SMT MB AB511 Z5W1M UMA 1.86G	N2920@/EMC@/AMIC@/LVDS@/DBG@/TPM@/PCB@/TS@
4319TDBOL03	SMT MB AB511 Z5W1M UMA 1.86G EPD HDMI	N2920@/EMC@/AMIC@/EDP@/DBG@/TPM@/PCB@/TS@
4319TDBOL04	SMT MB AB511 Z5W1M UMA 2.17G LVDS HDMI	N3520@/EMC@/AMIC@/LVDS@/DBG@/TPM@/PCB@/TS@
4319TDBOL05	SMT MB AB511 Z5W1M UMA 2.13G EPD HDMI	N2820@/EMC@/AMIC@/EDP@/DBG@/TPM@/PCB@/TS@
4319TDBOL06	SMT MB AB511 Z5W1M UMA 2.13G LVDS HDMI	N2820@/EMC@/AMIC@/LVDS@/DBG@/TPM@/PCB@/TS@
435MNVBOL01	SMT IO/B SB471 Z5W1M	EMC@

BOM Option Table

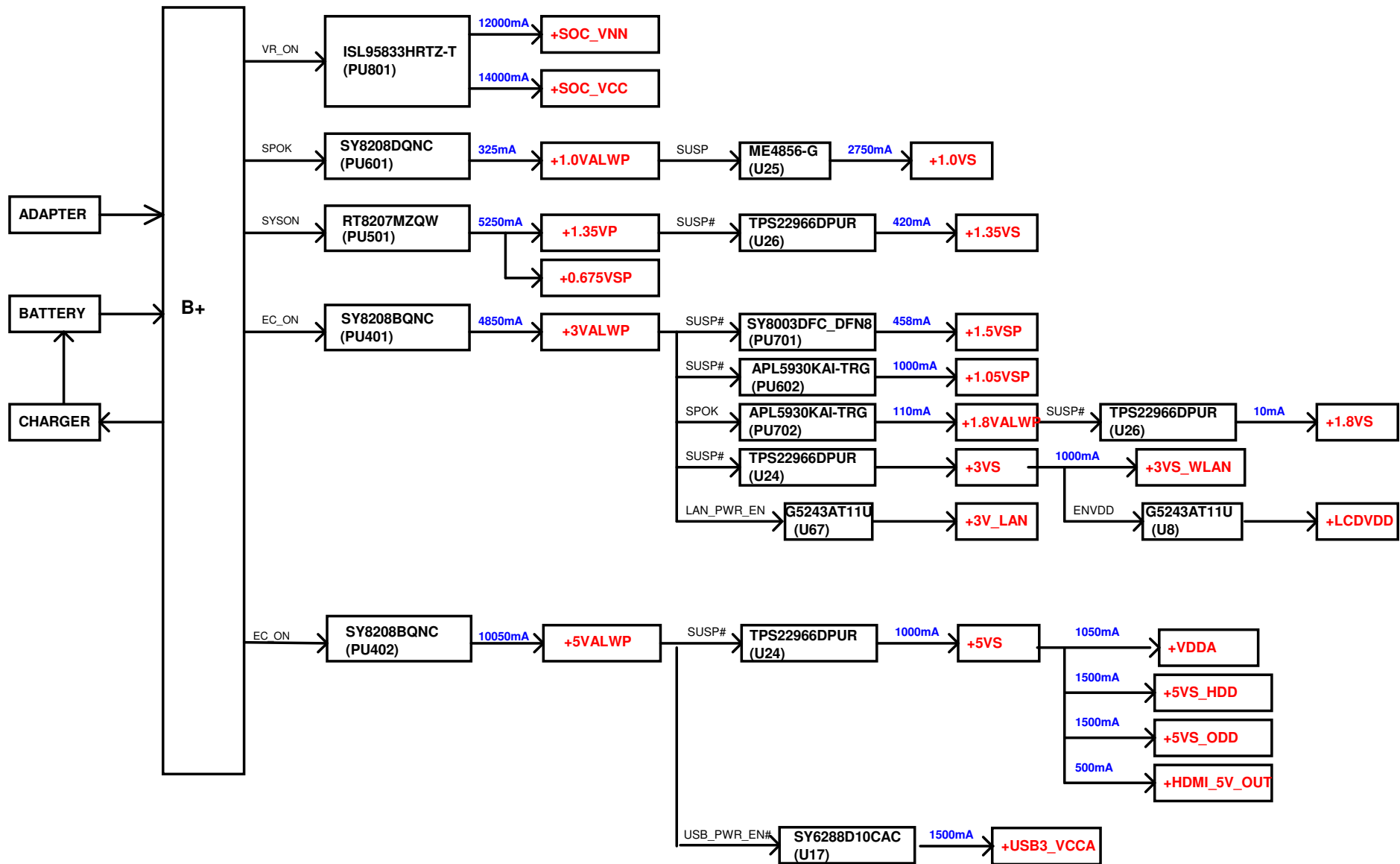
Item	BOM Structure
Unpop	@
Connector	CONN@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
IOAC support	AC@
Choose Analog MIC pop	AMIC@
Backlight Keyboard	BL@
EDP panel select	EDP@
LVDS panel select	LVDS@
Power Switch on board	DBG@
Jump for transfer power	JP@

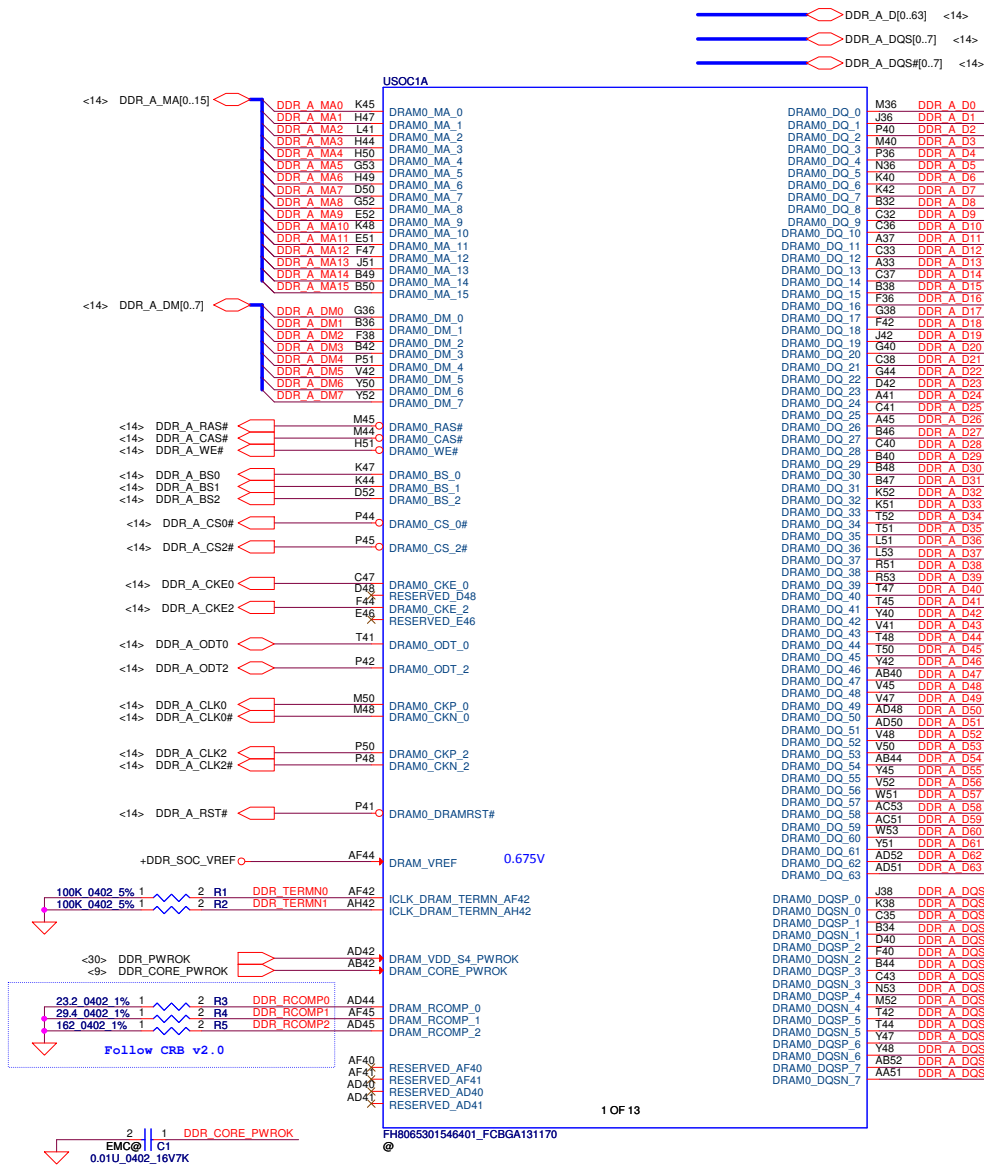
BOM Option Table

Item	BOM Structure
CPU for N2920 pop	N2920@
CPU for N3520 pop	N3520@
TPM support	TPM@
No supoort TPM	NTPM@
PCB PN	PCB@
CLEAN CMOS JUMP	SP@
Touch Screen function	TS@
EDP + Touch Screen	ETS@

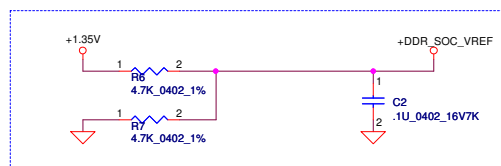


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				Date	Thursday, March 13, 2014
				Sheet	4 of 39
				Rev	1.0





Close To SOC Pin

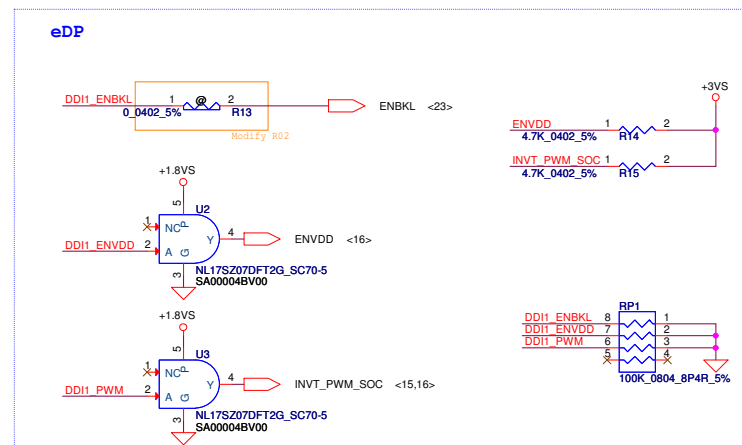
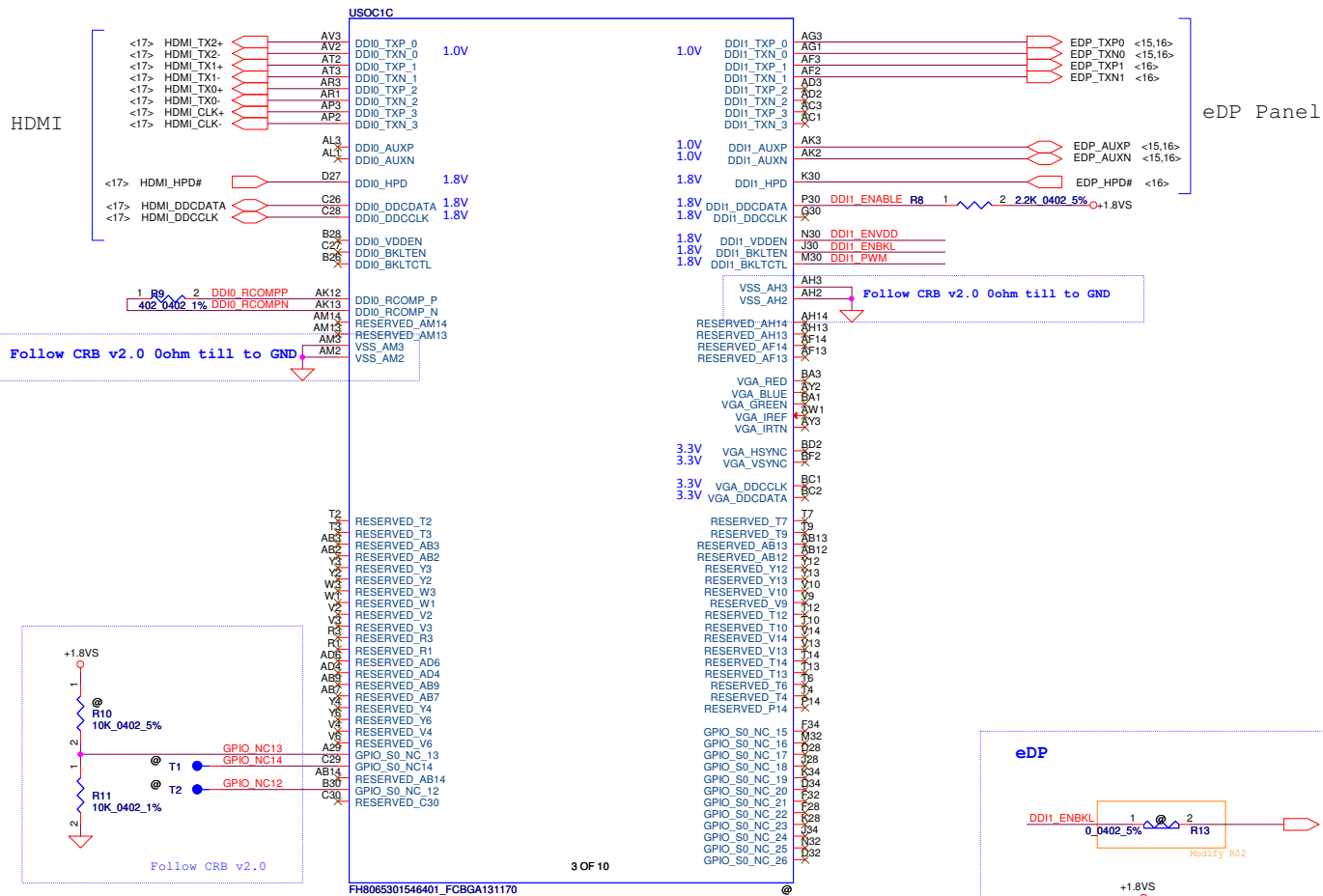


USOC1  
N3530@  
S IC FH8065301728500 QG9T C0 2.17G FCBGA  
Part Number = SA00007QG70

USOC1  
N2830@  
S IC FH8065301729601 QG9V C0 2.17G ABOI  
Part Number = SA00007QR30

USOC1  
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Part Number = SA00007R770

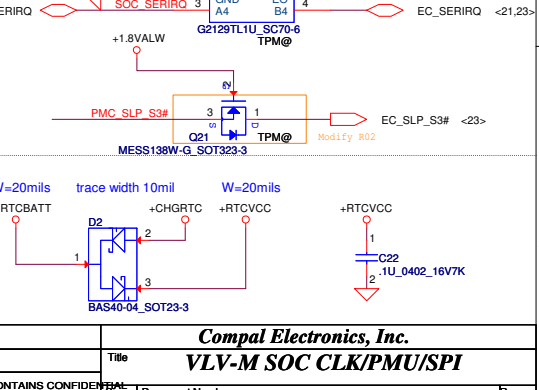
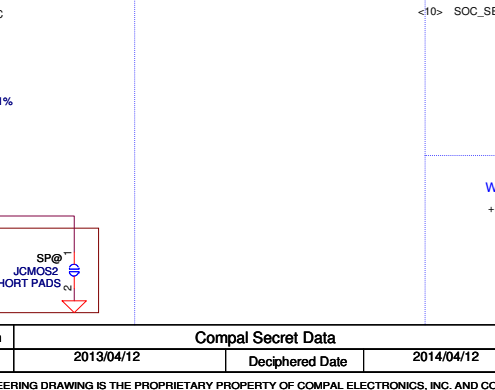
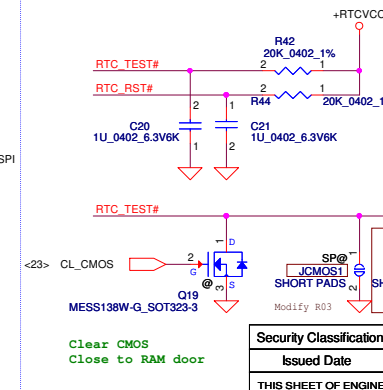
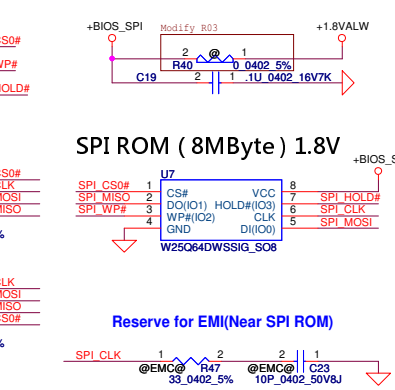
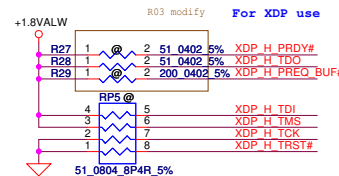
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	VLLV-M SOC Memory DDR3L	
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				Bay Trail M LA-B511P	1.0
				Date: Thursday, March 13, 2014	Sheet 6 of 39



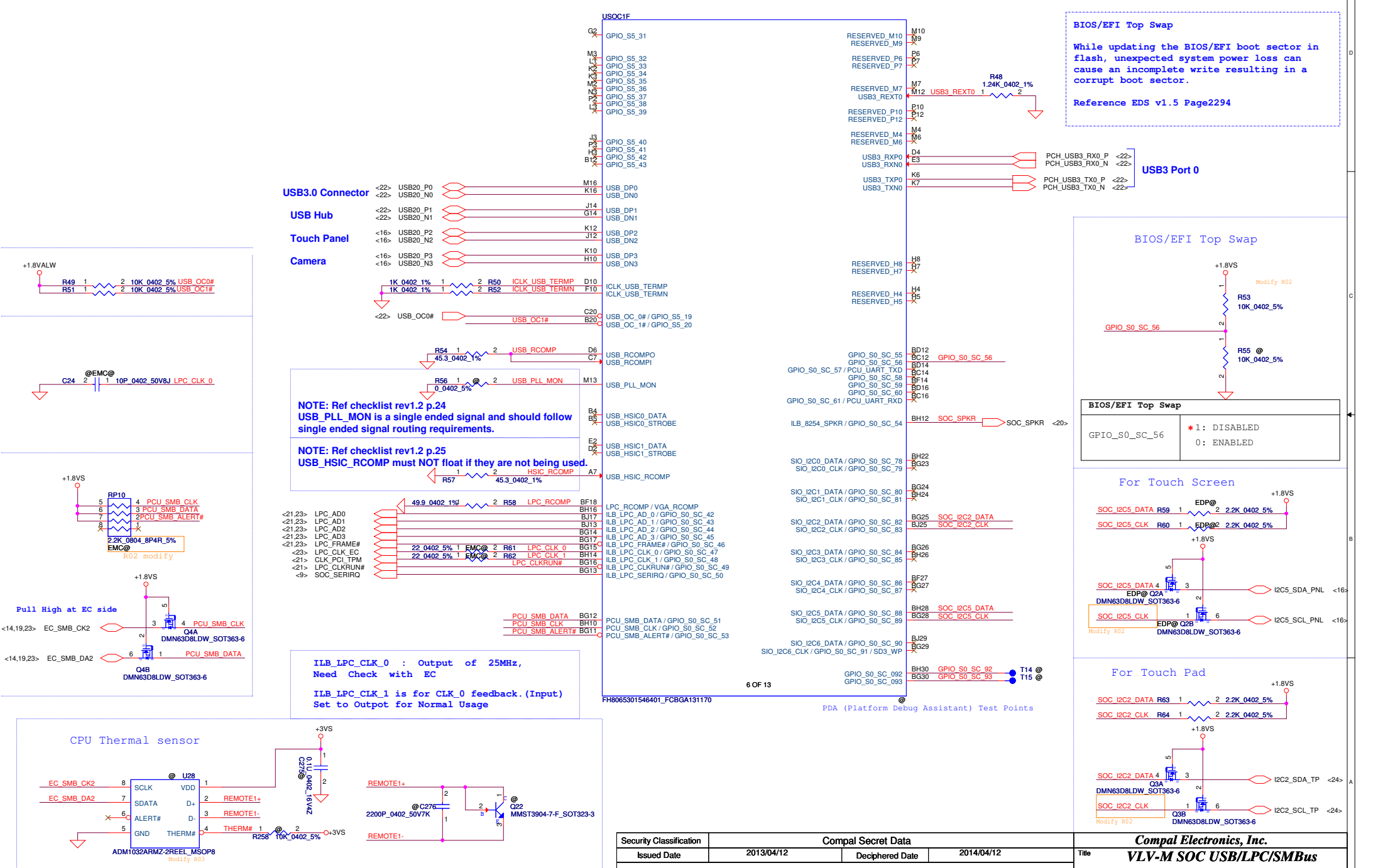
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				Date	Thursday, March 13, 2014
				Sheet	7 of 39
				Rev	1.0







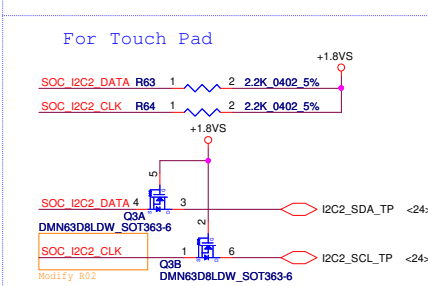
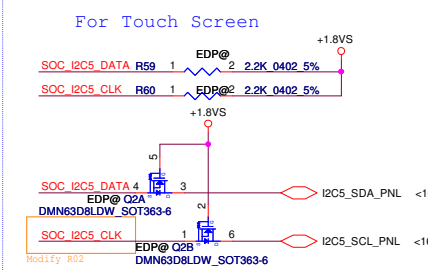
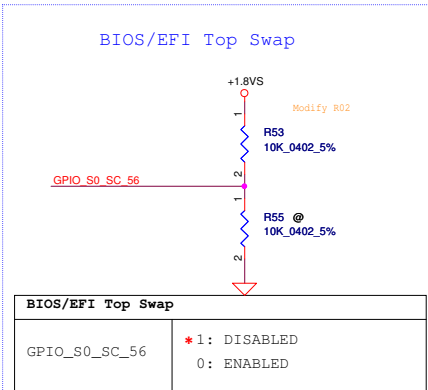
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				Customer	1.0	
				Bay Trail M LA-B511P		
				Date:	Thursday, March 13, 2014	Sheet



BIOS/EFI Top Swap

While updating the BIOS/EFI boot sector in flash, unexpected system power loss can cause an incomplete write resulting in a corrupt boot sector.

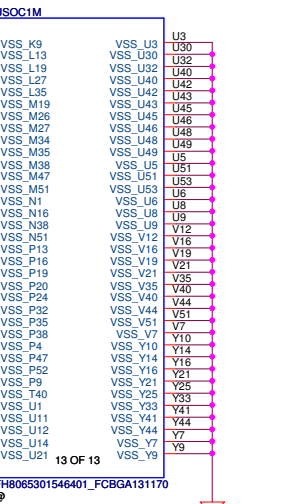
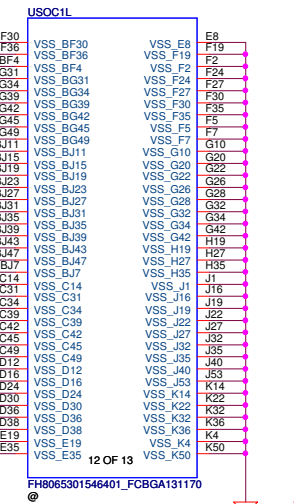
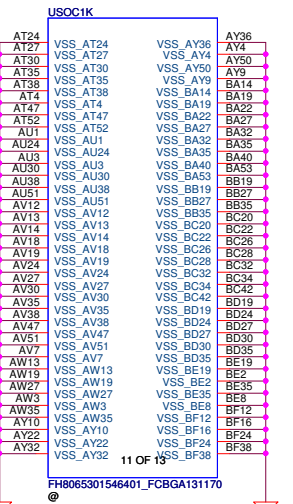
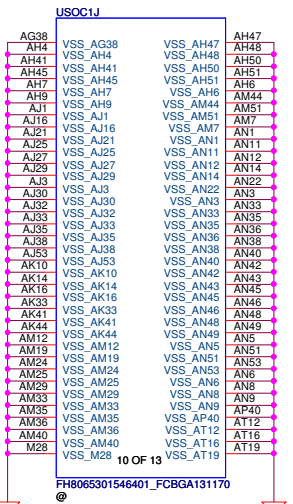
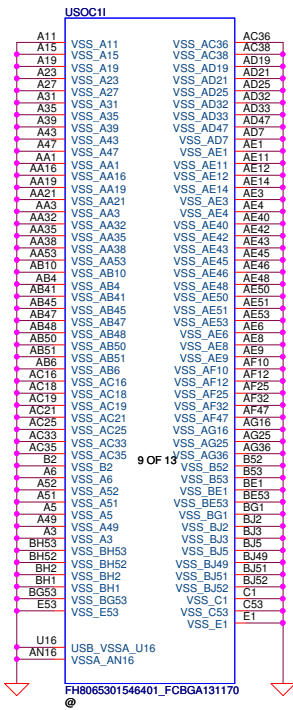
Reference EDS v1.5 Page2294

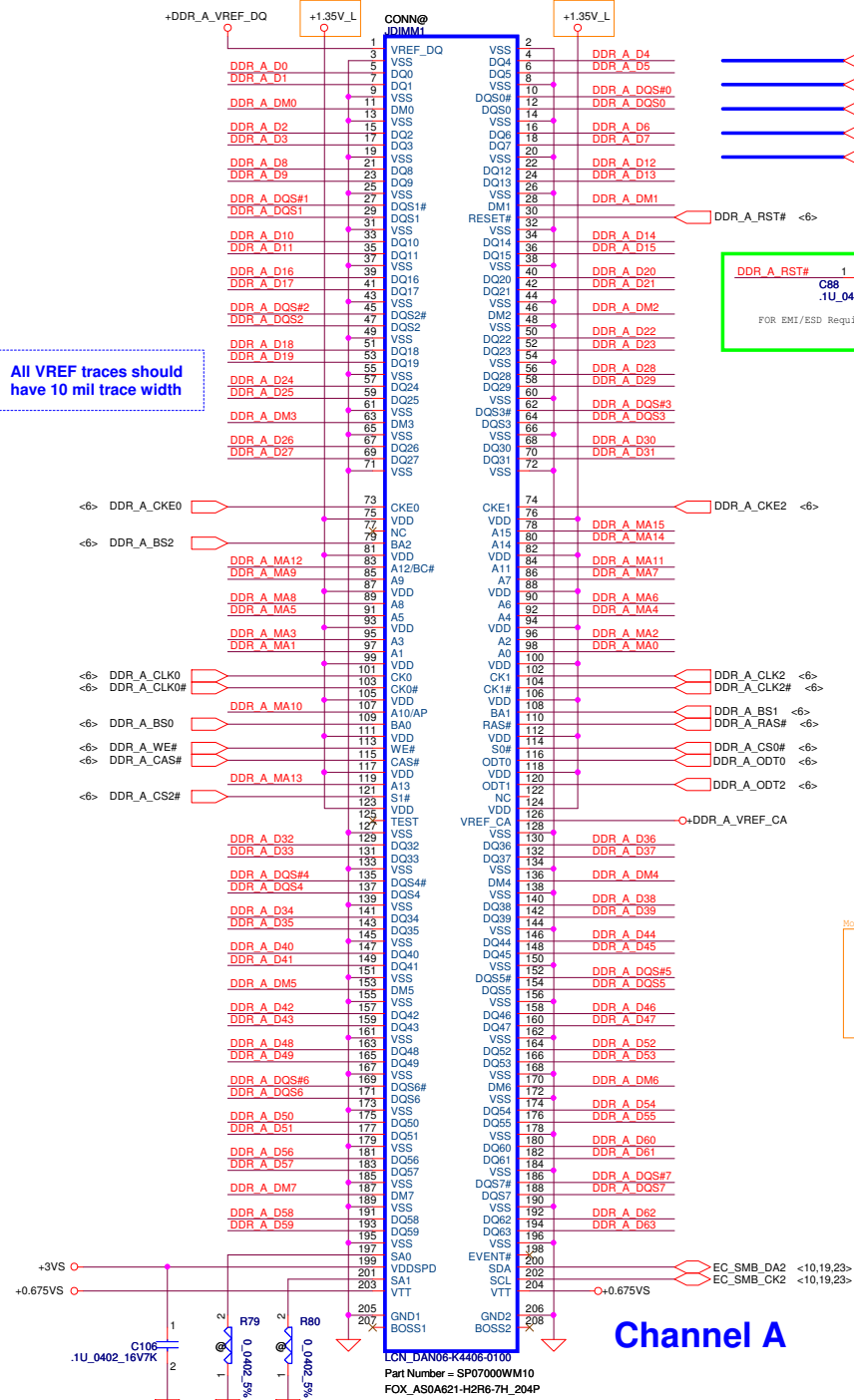


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Customer				Bay Trail M LA-B511P
Date				Thursday, March 13, 2014
Sheet				10 of 39









Channel A

<Address: SA1:SA0=00 (A0H)>  
DIMM\_1 STD H:4mm

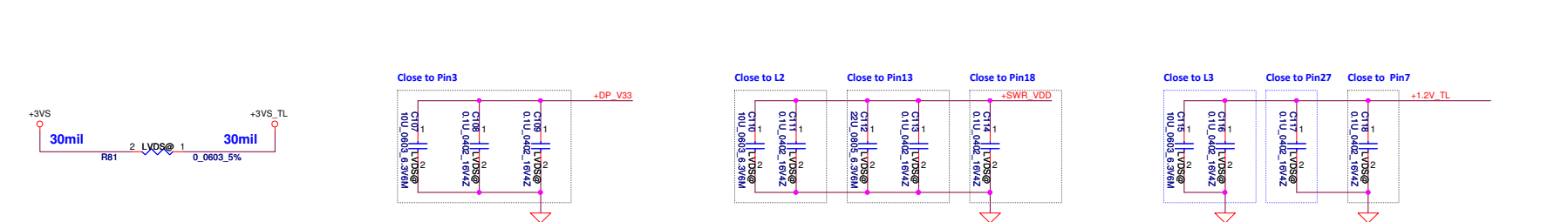
Signal voltage level = 0.675 V  
PLACE TWO 4.7K RESISTORS CLOSE TO  
DIMMS ON DIMM\_VREF\_CA / DIMM\_VREF\_DQ  
Decoupling caps are needed; one 0.1 uF placed close to VREF pins of each DDR3 SODIMM.

Layout Note:  
Place near JDIMM1

Layout Note:  
Place near JDIMM1.203,204

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				Bay Trail M LA-B511P	1.0
				Date: Thursday, March 13, 2014	Sheet 14 of 39

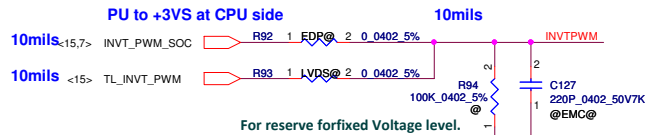
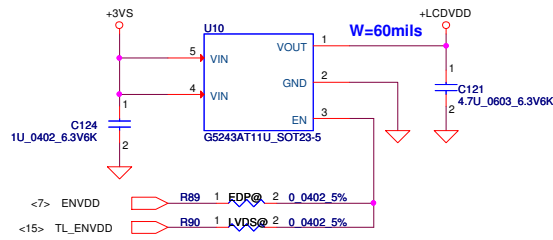
A	B	C	D	E
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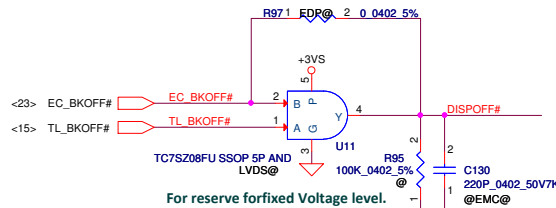
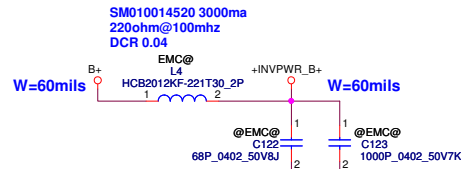
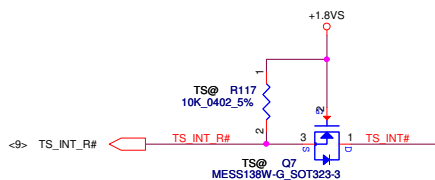
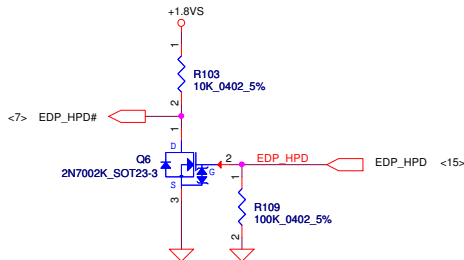
		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE*	EEPROM MODE



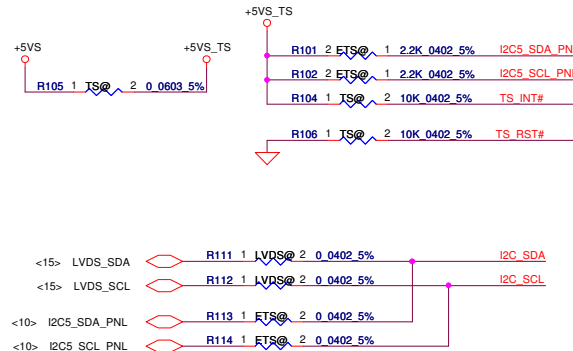
## LCD POWER CIRCUIT



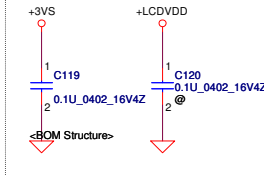
Intel recommends having a pull-up resistor of 100 kΩ for AUXN and a pull-down resistor of 100 kΩ for AUXP between the AC capacitor and the connector, to assist source detection by the sink device.  
All reverse on before project.



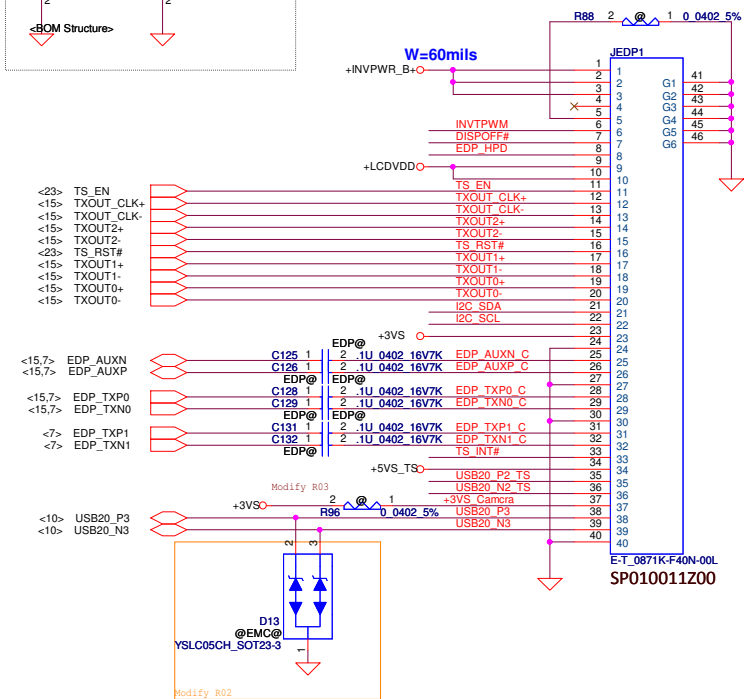
For Select LVDS EDID or EDP I2C touch



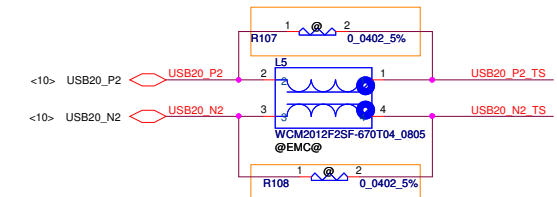
Place closed to JLVDS1



## LCD/ LED PANEL Conn.



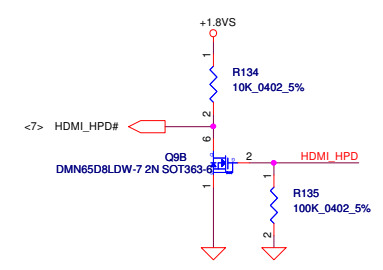
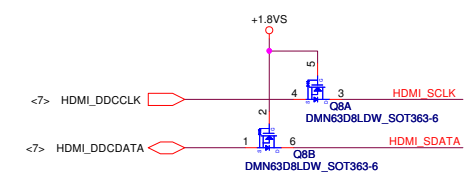
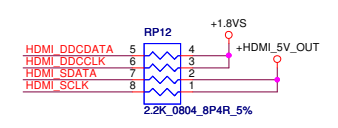
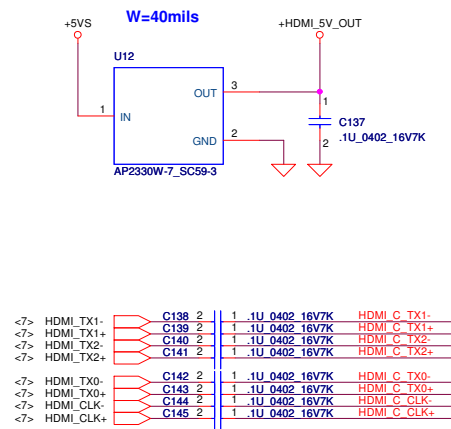
Touch



Solution	Panel	Touch	BOM option
Cable 1	eDP	I2C,USB	EDP@,TS@
Cable 2	LVDS	USB	LVDS@

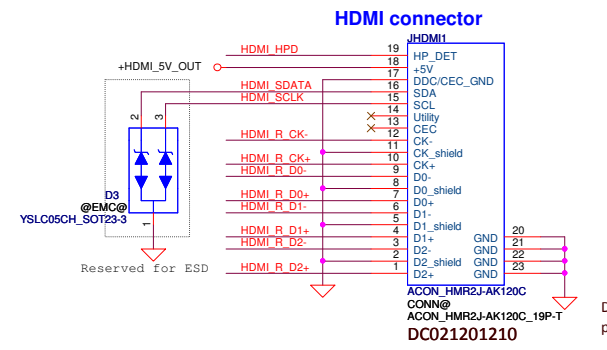
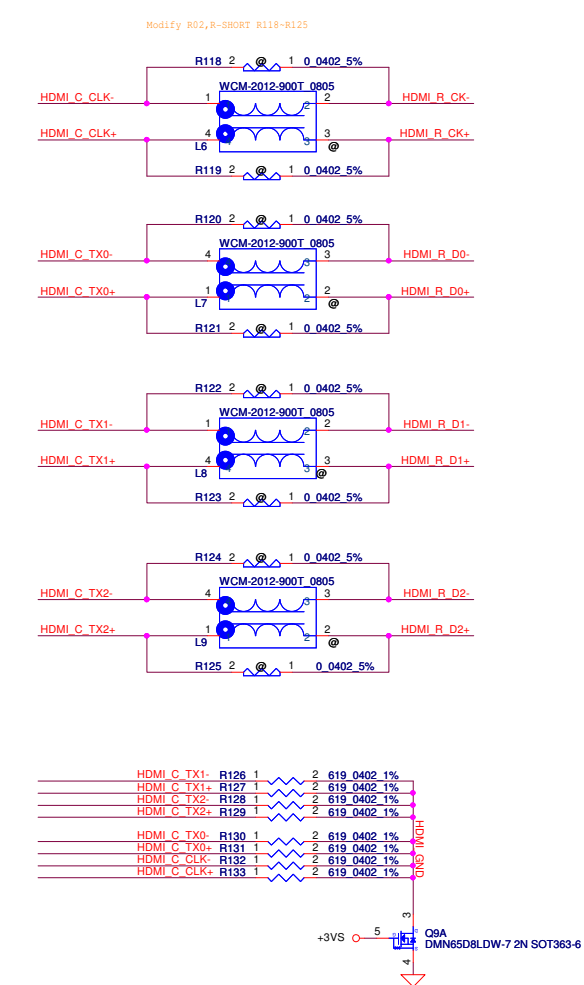
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Deciphered Date				2014/04/12				eDP CONN.			
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Date:				Thursday, March 13, 2014				Rev			
Sheet				16				of			
99											



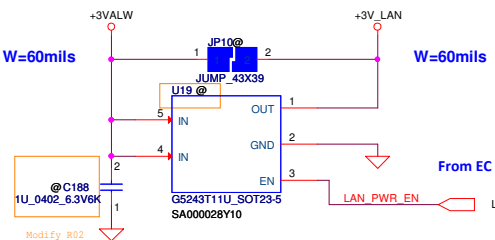


ZZZ

HDMI\_ROYALTY  
ROYALTY HDMI W/LOGO+HDCP  
R00000003HM  
45@



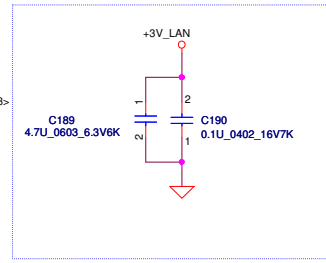
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Bay Trail M LA-B511P				Date: Thursday, March 13, 2014 Sheet 17 of 39



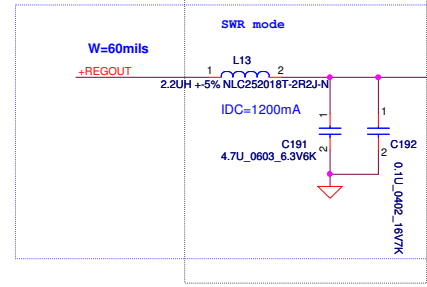
+3V\_LAN Rising time request: 0.5~100ms

SA000028Y10  
High active.  
EN threshold voltage :1.2~2.0V  
Current limit threshold :1.5~2.8A  
Output turn-on rising time: 1.3~2.7ms

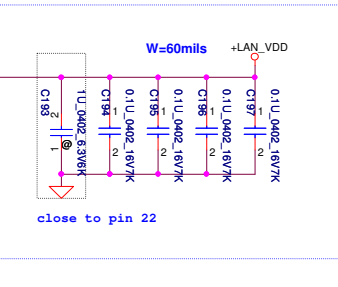
Close to U20 Pin23



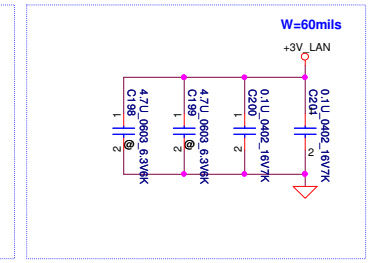
( Should be place within 200 mils )  
Close to Pin 24



Close to Pin 3,8,22,30  
1uF reserved for Pin 22

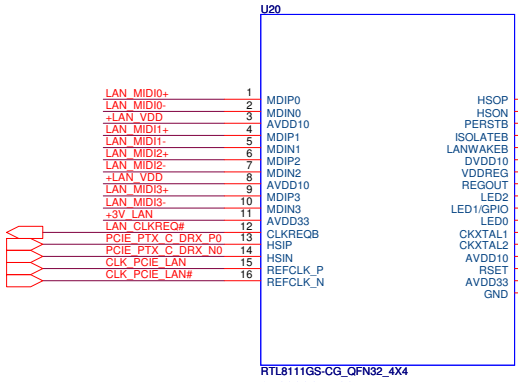


Close to Pin 11,32



PU to +3VS at PCH side

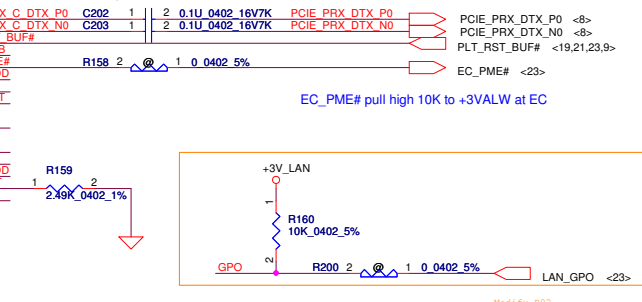
<8> LAN\_CLKREQ#  
<8> PCIE\_PTX\_C\_DRX\_P0  
<8> PCIE\_PTX\_C\_DRX\_N0  
<9> CLK\_PCIE\_LAN  
<9> CLK\_PCIE\_LAN#



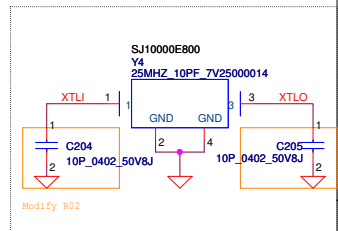
RTL8111GS-CG\_OFN32\_4X4  
SA00006ML00

Use 8111GS symbol , pop 8111GUS part

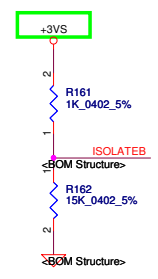
close to Pin 17, 18



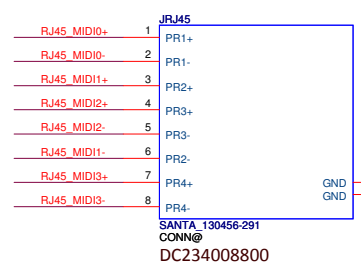
EC\_PME# pull high 10K to +3VALW at EC



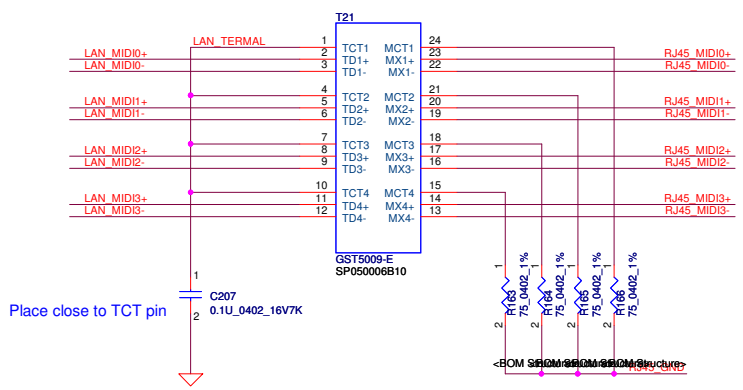
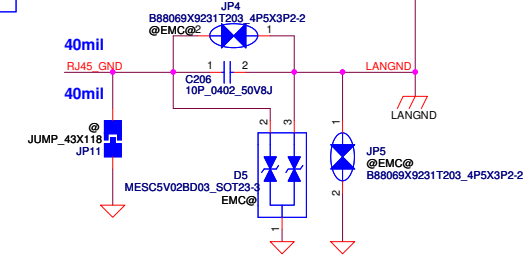
Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S3~S5.



LAN Connector

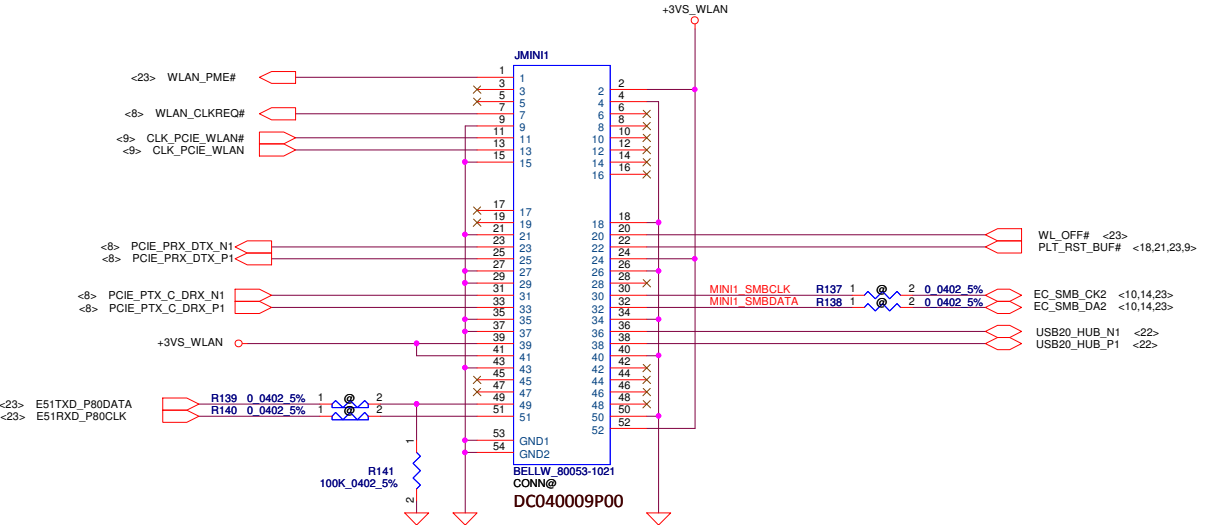
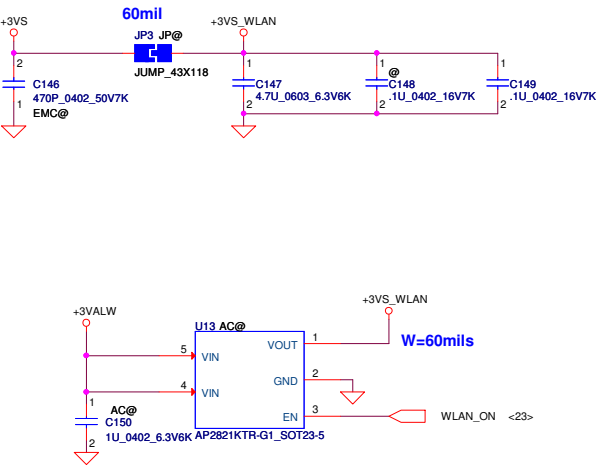


SANTA 130456-291  
CONING@  
DC234008800



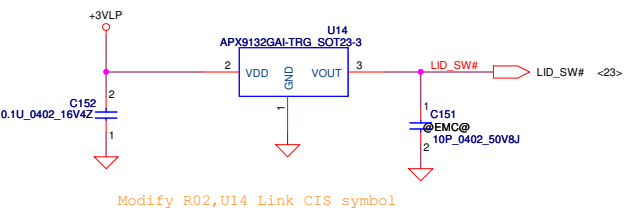
Place close to TCT pin

For Wireless LAN



Hall sensor

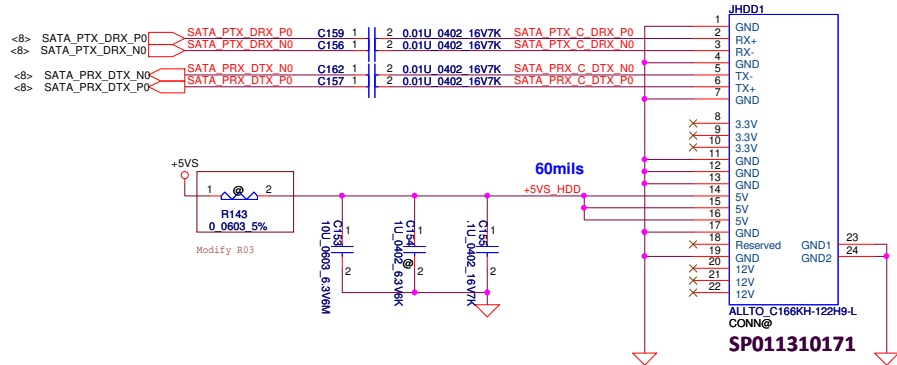
Lid Switch  
(Hall Effect Switch)



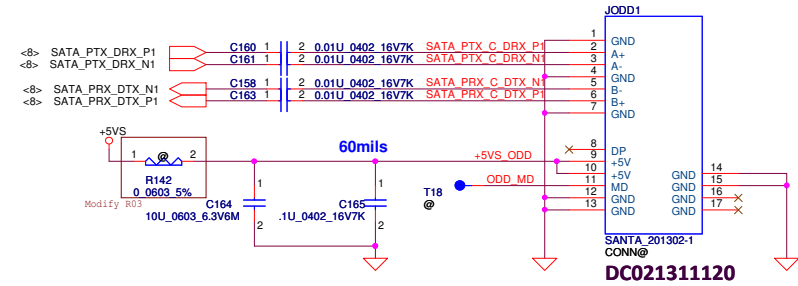
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	Mini PCIE(WLAN)
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				Date	Thursday, March 13, 2014
				Sheet	19 of 39



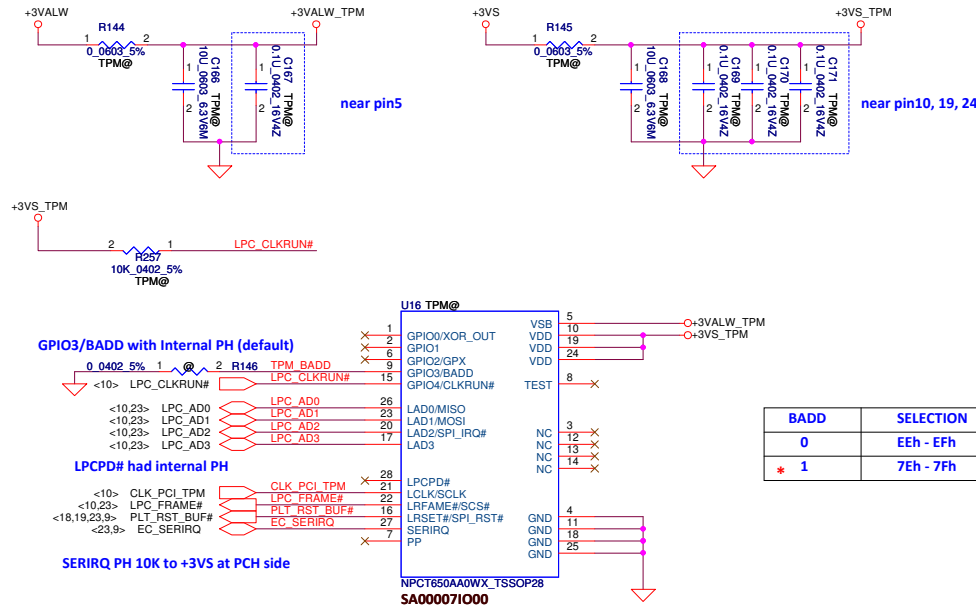
## SATA HDD1 Conn.



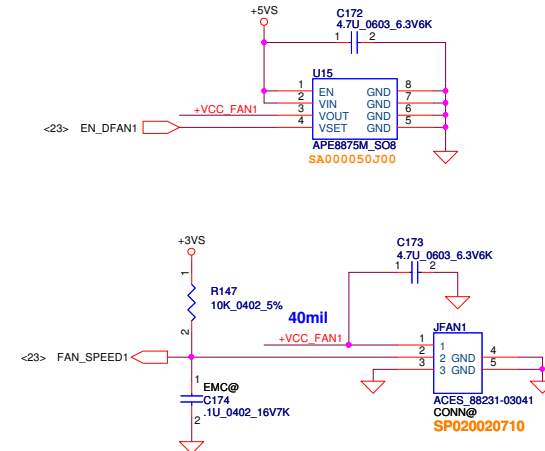
## SATA ODD Conn.



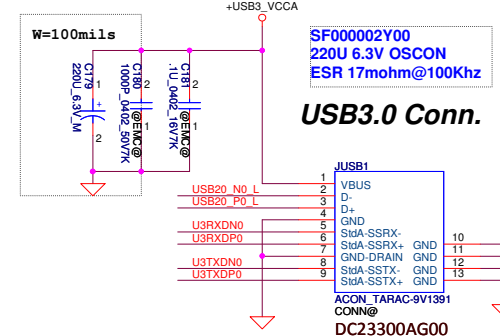
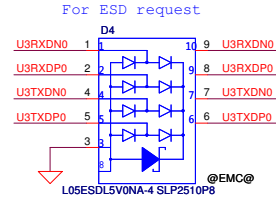
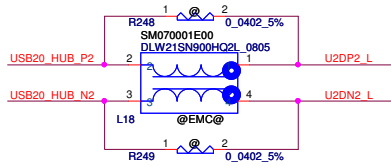
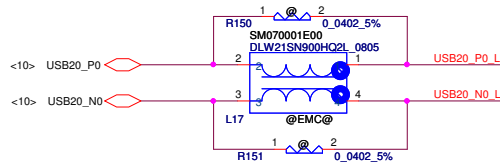
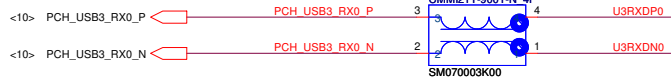
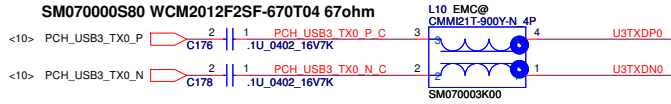
## TPM



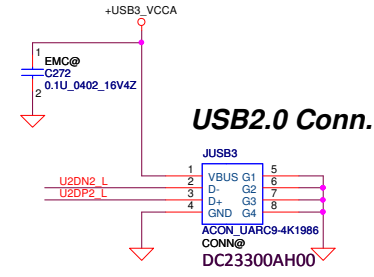
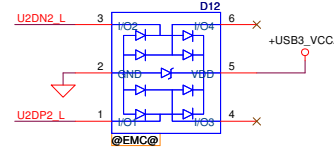
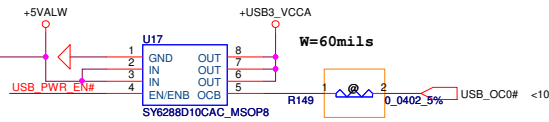
## FAN1 Conn



# USB3.0 (Port 0)

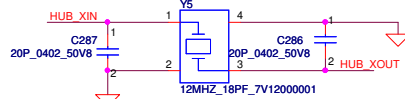
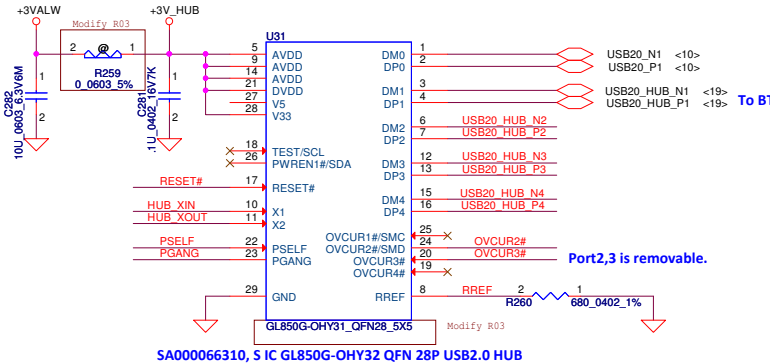
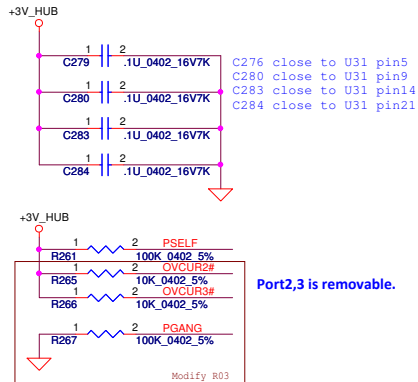


USB3.0 Conn.

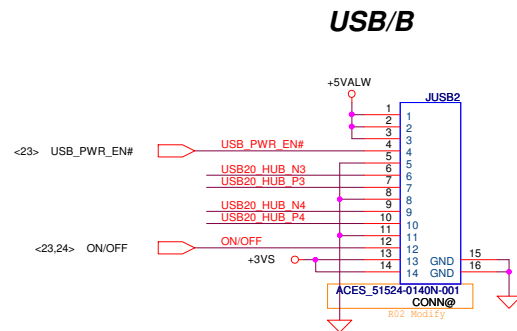


USB2.0 Conn.

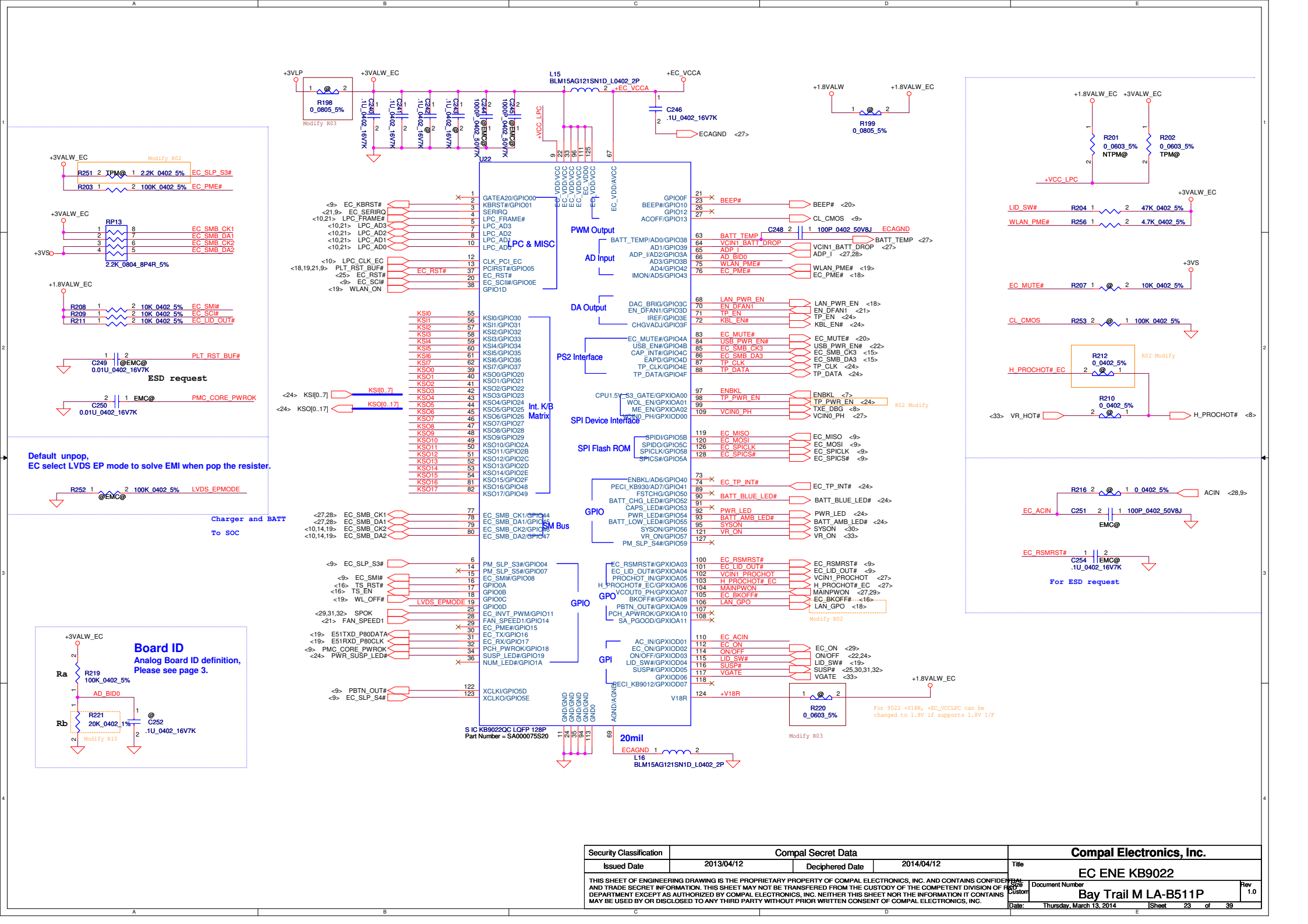
## USB\_HUB



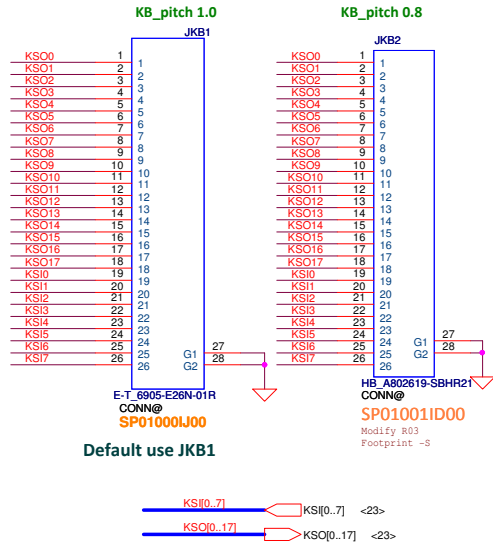
USB HUB Port  
Port1 BT  
Port2 USB2.0  
Port3 USB2.0  
Port4 Card Reader



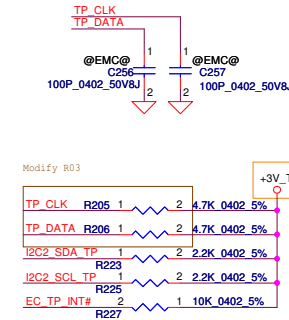
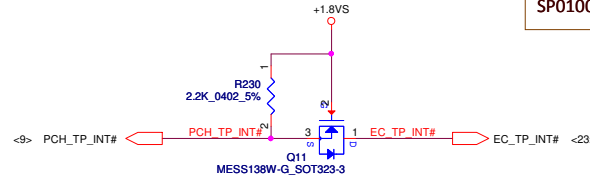
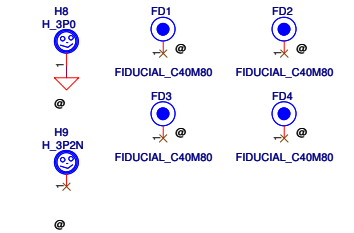
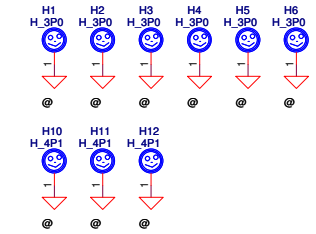
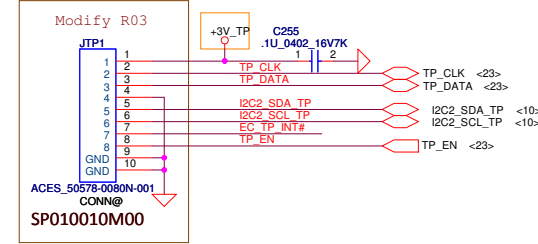
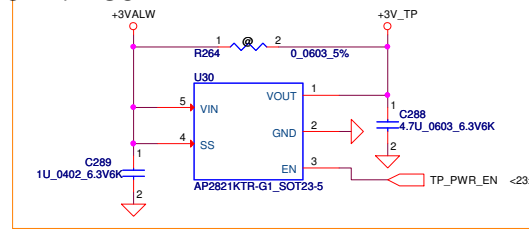
USB/B



## KB Conn.

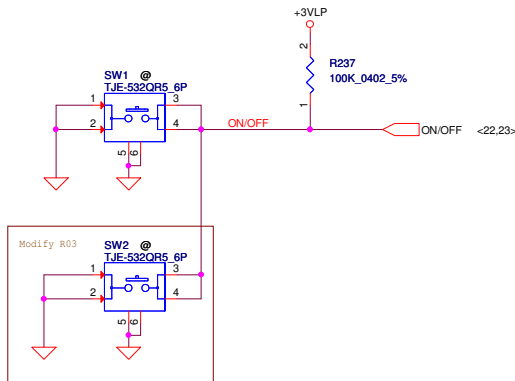


## To TP/B Conn.

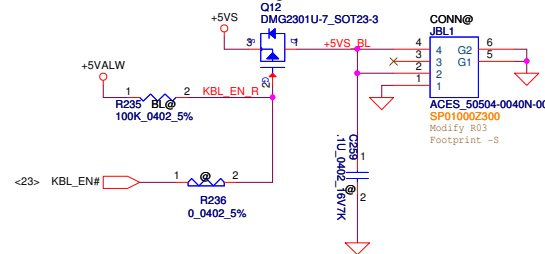


Event	PCH_TP_INT#	EC_TP_INT#
S0	Interrupt	X
S3	X	Wake
1. Clamshell closed or Lid closed	X	X
2. Tablet mode for Convertible design	X	X
3. Disable TP function by hot-key	X	X

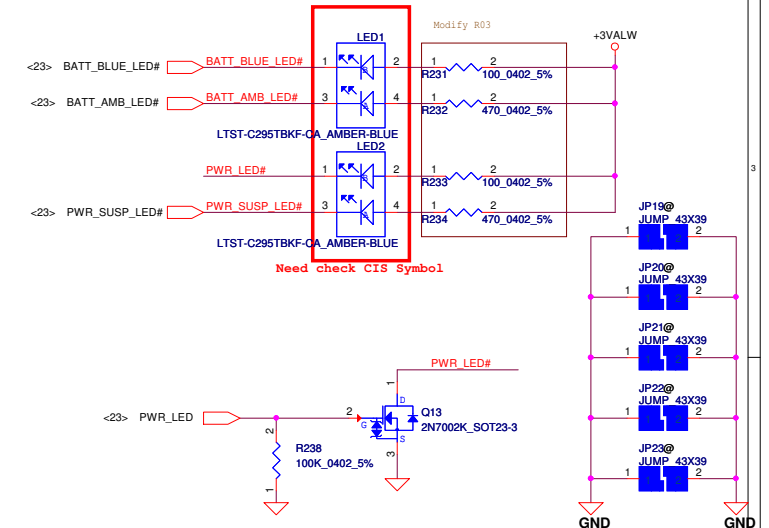
## ON/OFF BTN



## KB BackLight Conn.



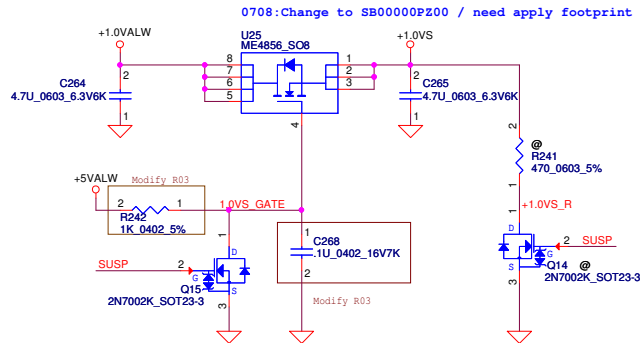
## LED



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Date: Thursday, March 13, 2014				Sheet 24 of 39

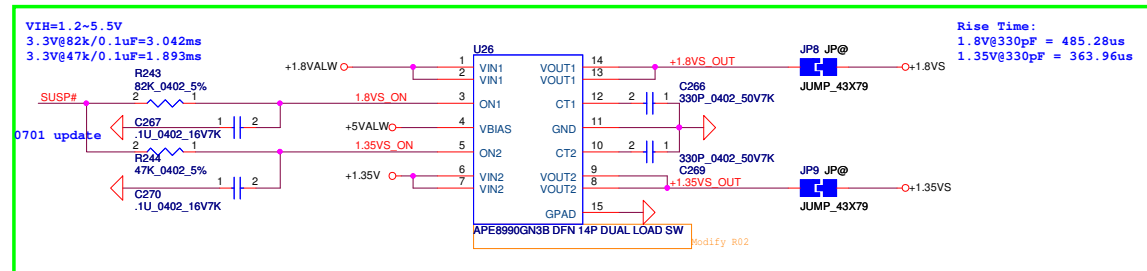
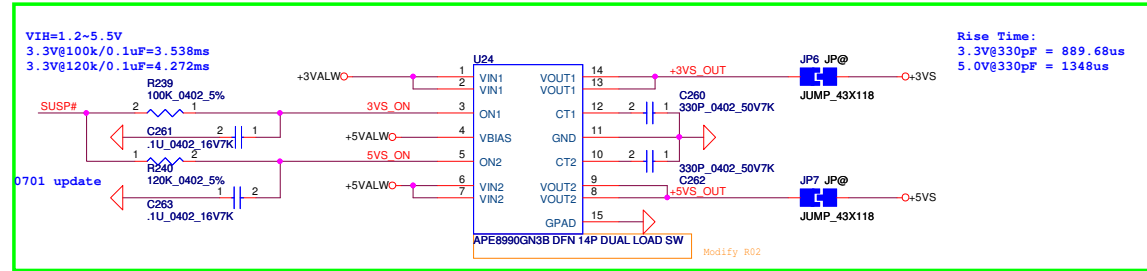
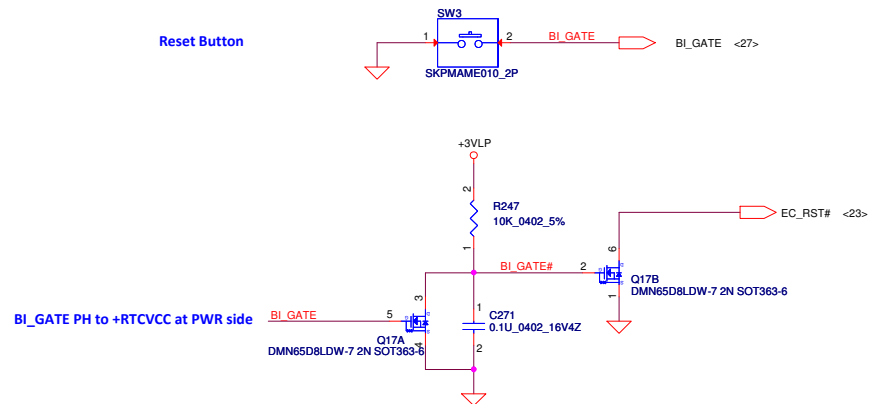


## +1.0VALW TO +1.0VS

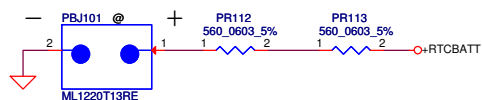
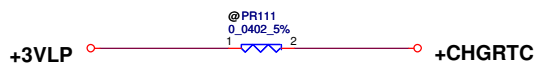
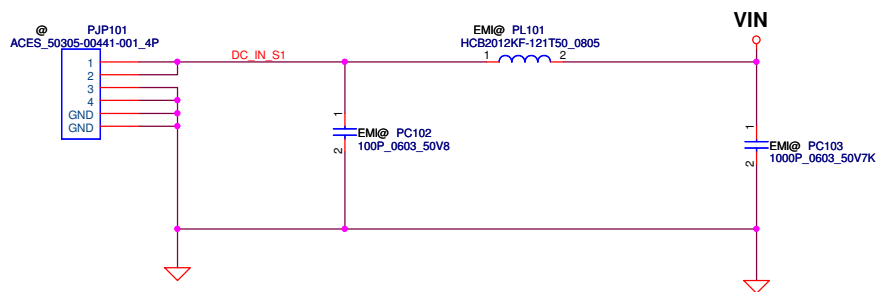


## Reset Button / Battery discharge screw hole

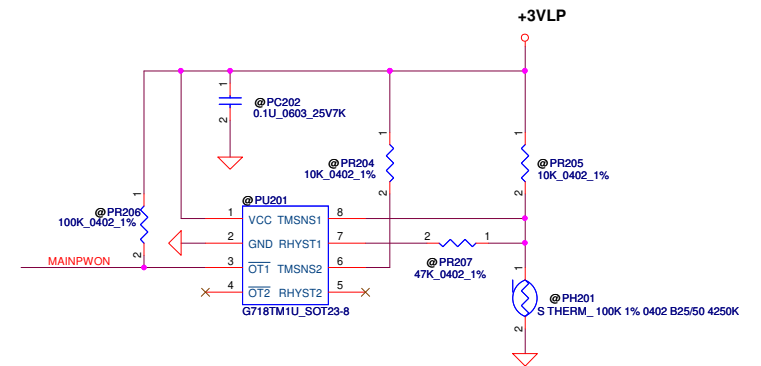
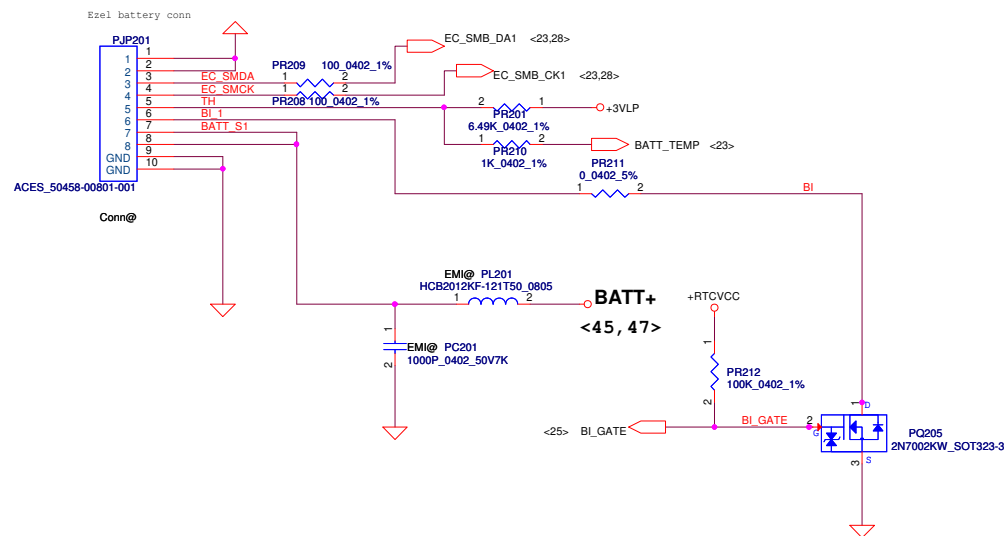
Follow VAS2\_HB design



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				Bay Trail M LA-B511P
				Rev 1.0
				Date: Thursday, March 13, 2014
				Sheet 25 of 39



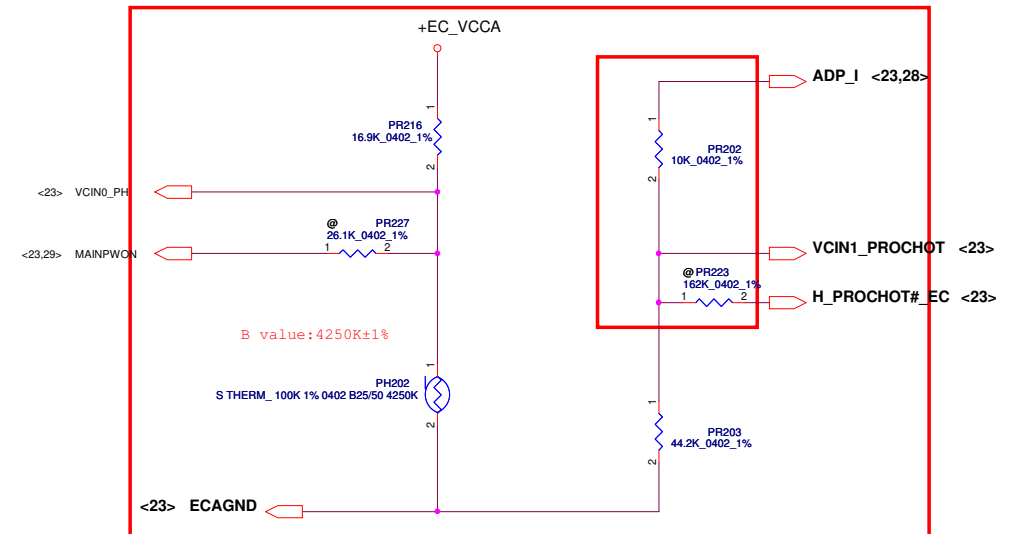
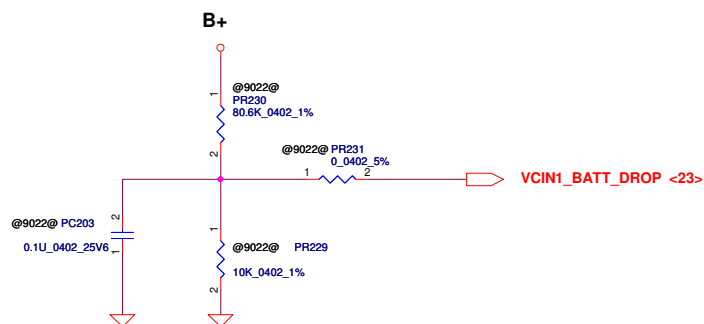
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				Custom	Bay Trail M LA-B511P	1.0
				Date:	Thursday, March 13, 2014	Sheet 26 of 39



	For KB9012 OTP	For KB9022 OTP
92°C	1.2V	1.0V
56°C	1.2V	1.0V
PR216	22.6K ohm	32.4K ohm
PR227	26.1K ohm	30.9K ohm

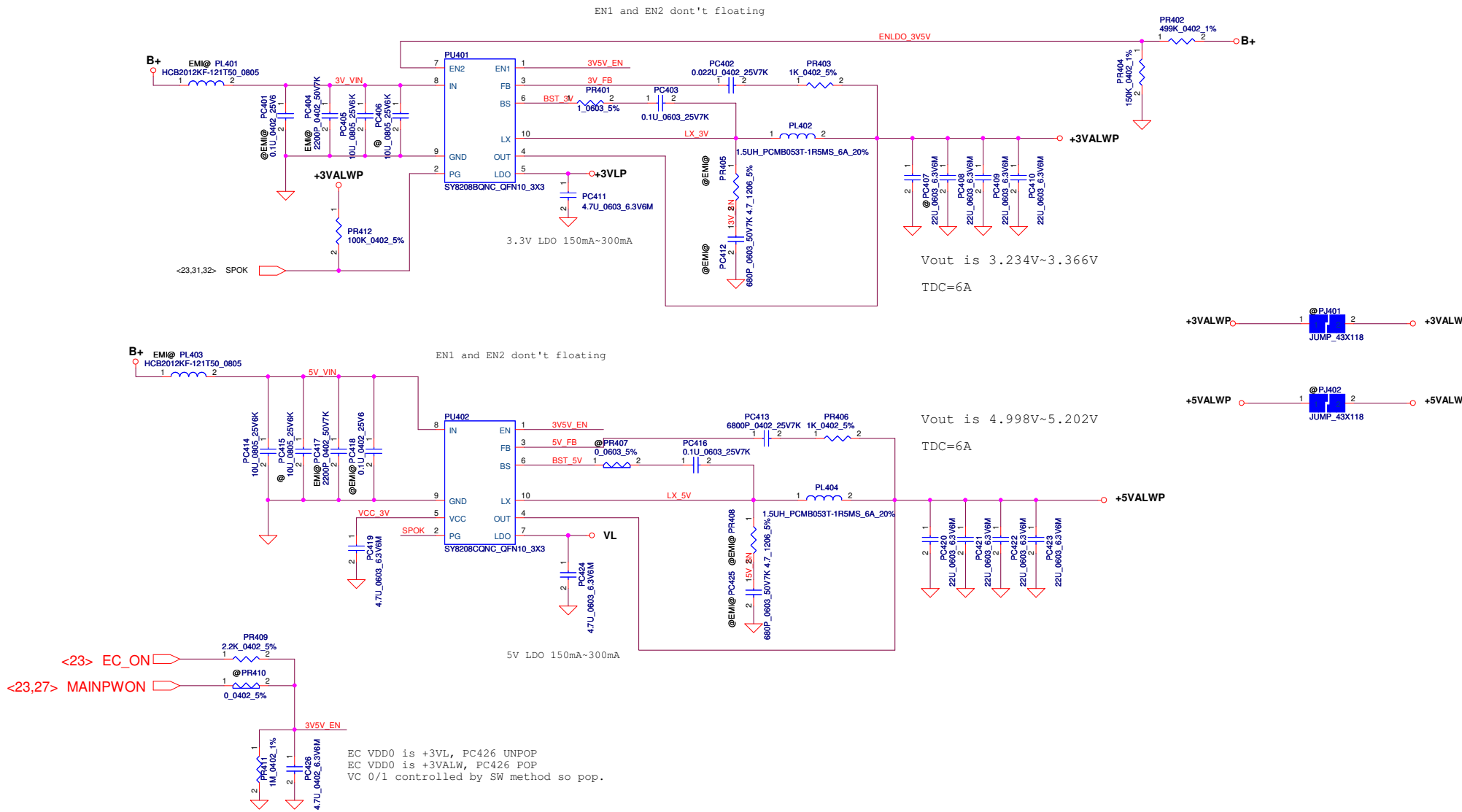
Need confirm the setting

For KB9022 sense 20mΩ	Active	Recovery
40W	42.8W, 0.43V	34.4W, 0.43V

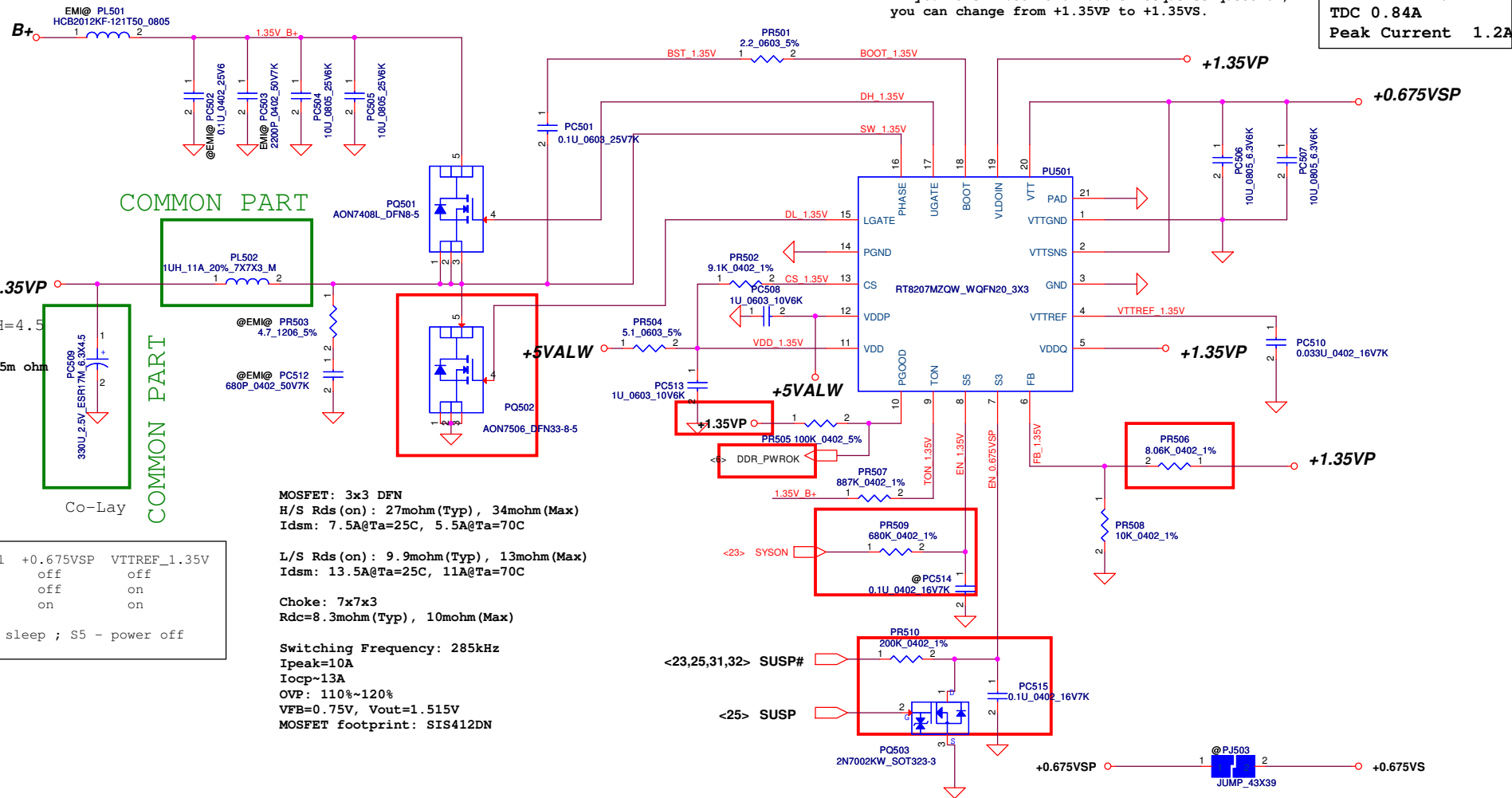


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						Custom		Bay Trail M LA-B511P		1.0	
Date:		Thursday, March 13, 2014		Sheet		27 of 39					





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				Date	Thursday, March 13, 2014
				Sheet	29 of 39
				Rev	1.0



SF000002Z00 H=4.5

ESR=15m ohm

Co-Lay

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

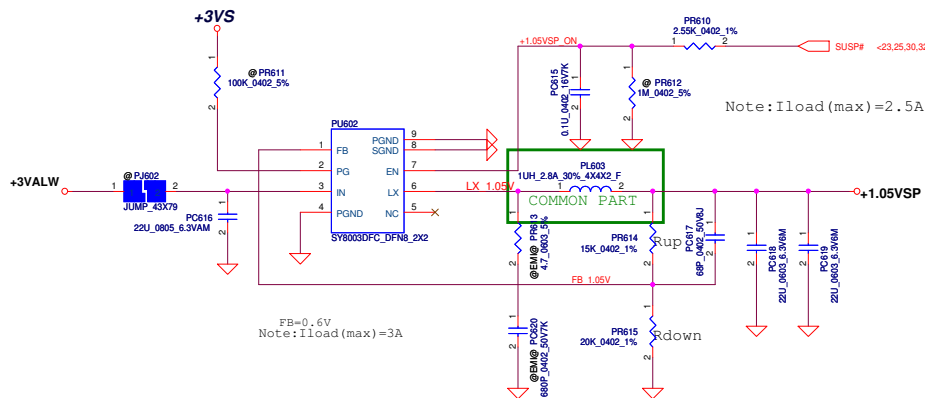
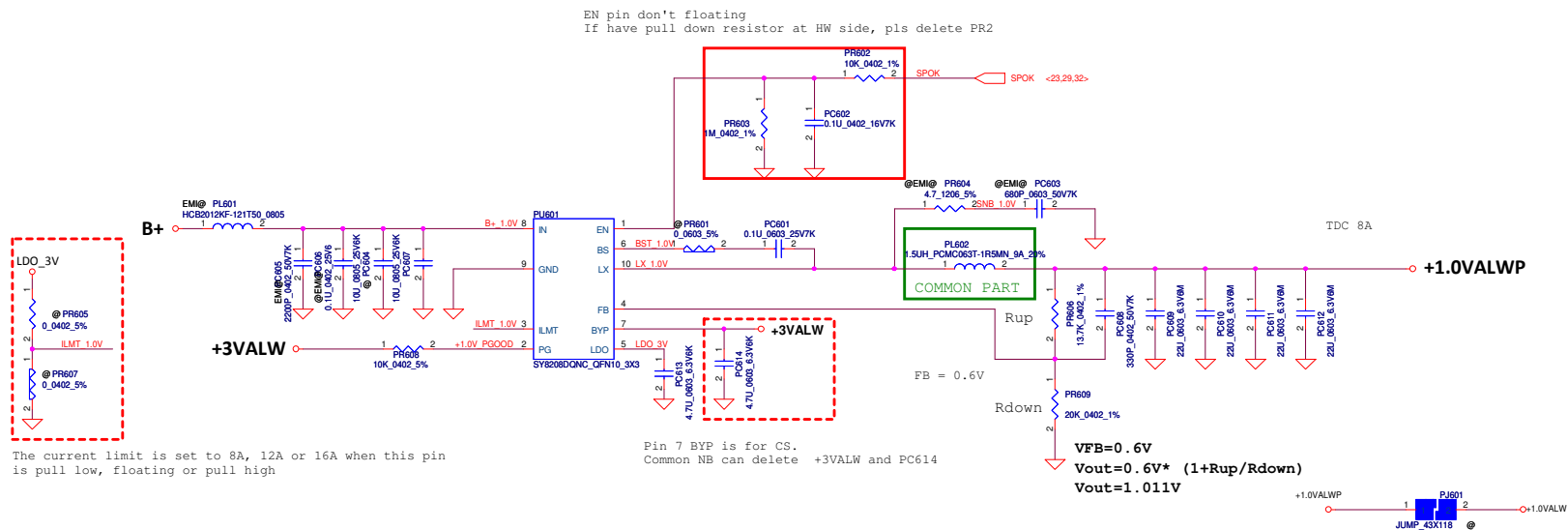
MOSFET: 3x3 DFN  
H/S Rds (on): 27mohm(Typ), 34mohm(Max)  
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds (on): 9.9mohm(Typ), 13mohm(Max)  
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

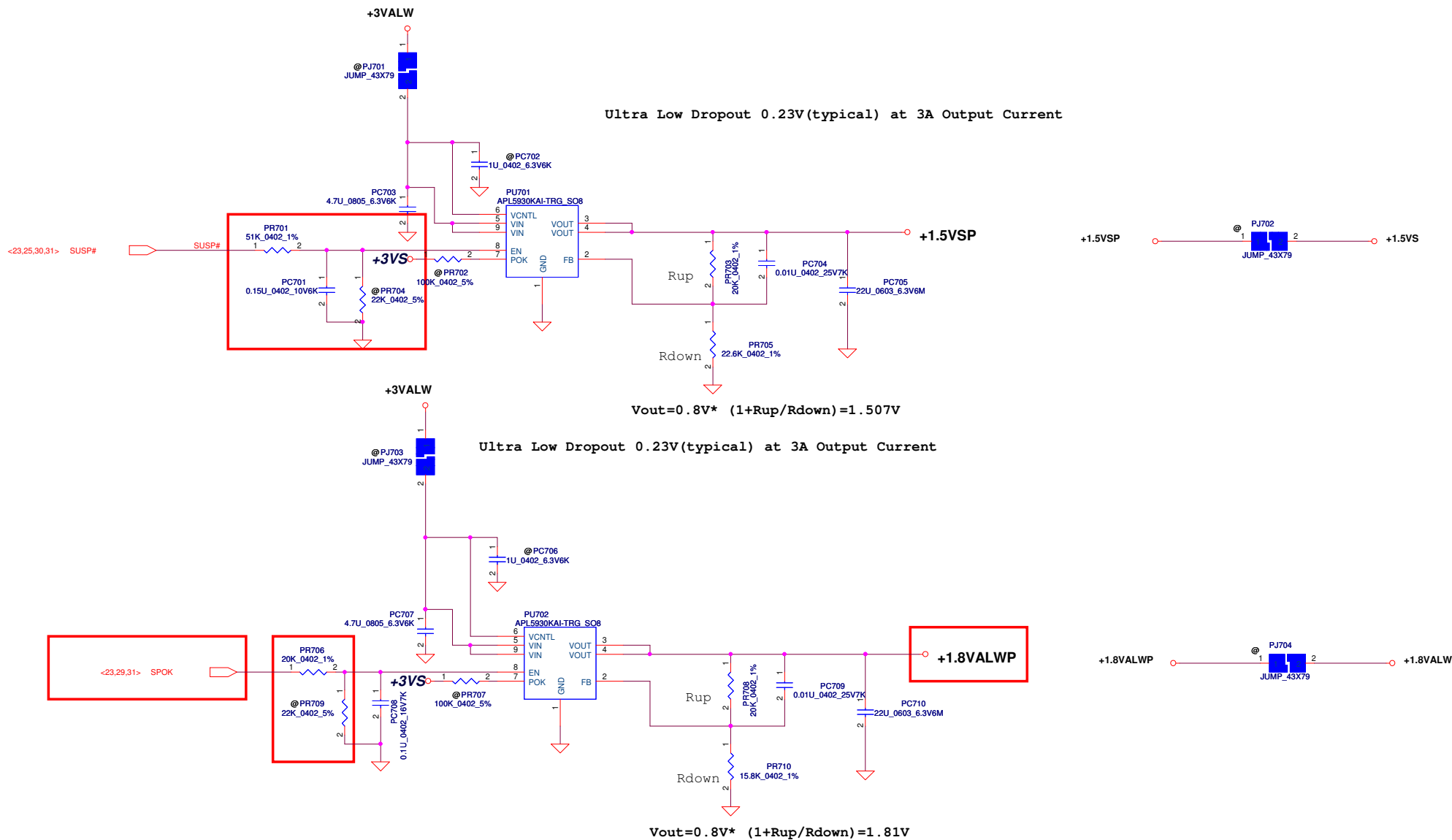
Choke: 7x7x3  
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz  
Ipeak=10A  
Iocp~13A  
OVP: 110%~120%  
VFB=0.75V, Vout=1.515V  
MOSFET footprint: SIS412DN

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				Custom	Bay Trail M LA-B511P
				Date	Thursday, March 13, 2014
				Sheet	30 of 39
				Rev	1.0



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				C	Bay Trail M LA-B511P	1.0
				Date:	Thursday, March 13, 2014	Sheet 31 of 39



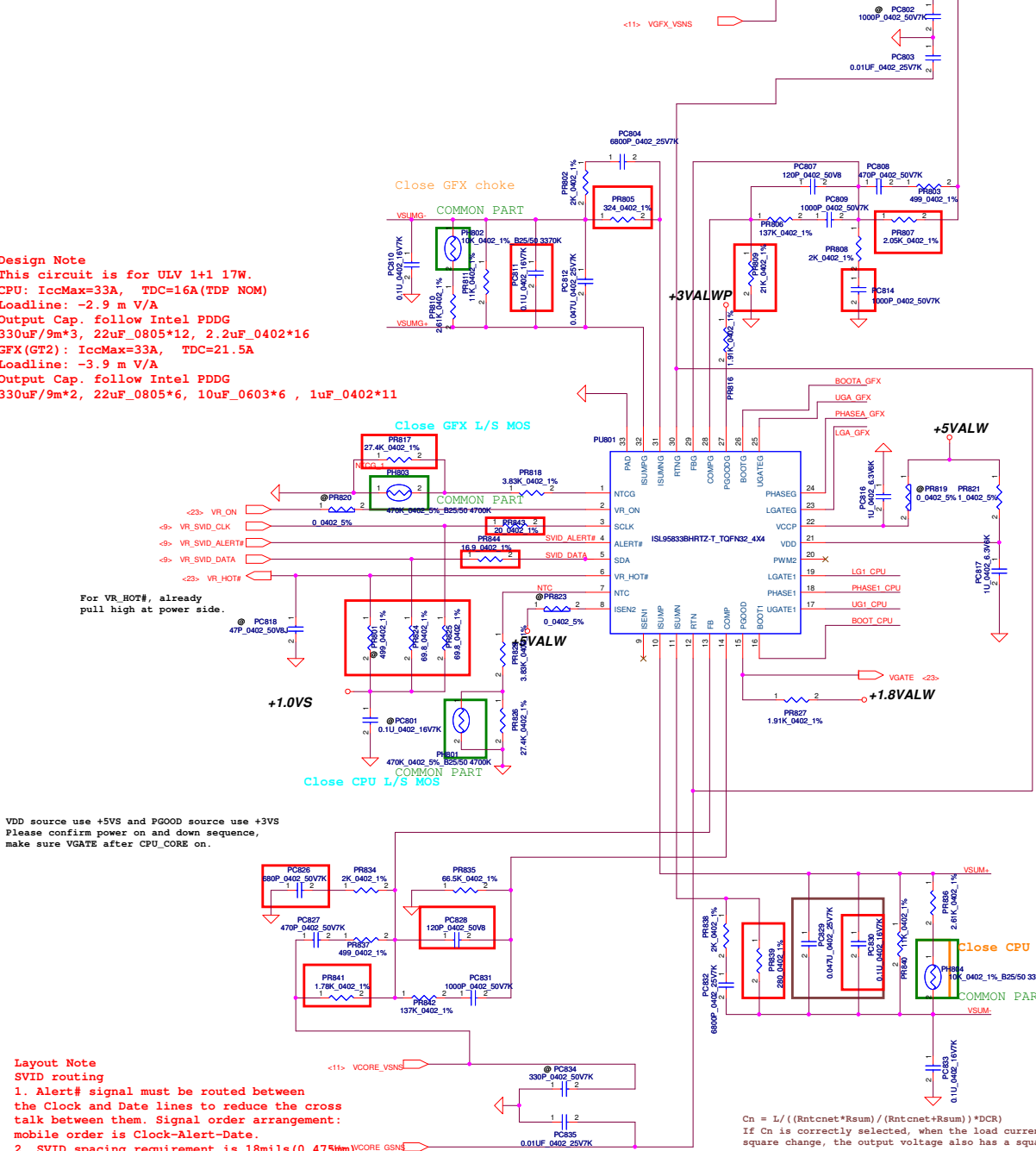
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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				Date	Thursday, March 13, 2014
				Sheet	32 of 39



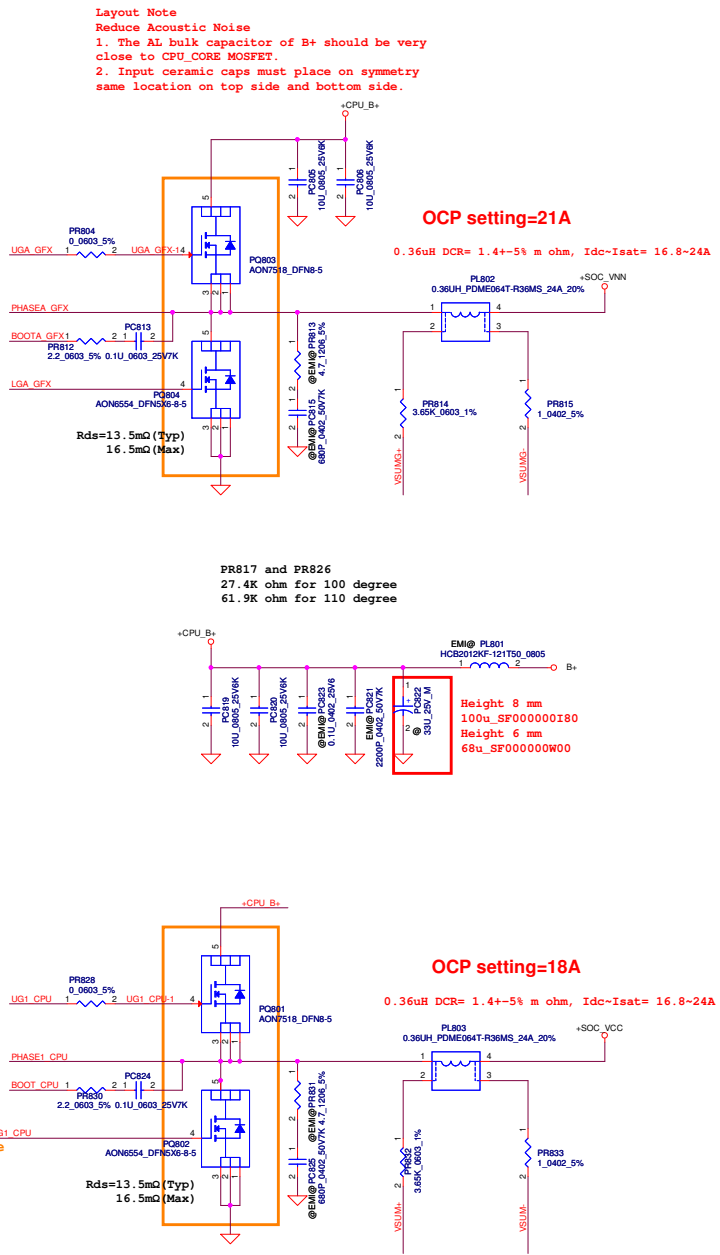
Design Note  
This circuit is for ULV i+1 17W.  
CPU: IccMax=33A, TDC=16A(TDP NOM)  
Loadline: -2.9 m V/A  
Output Cap. follow Intel PDDG  
330uF/9m\*3, 22uF\_0805\*12, 2.2uF\_0402\*16  
GFX(GT2): IccMax=33A, TDC=21.5A  
Loadline: -3.9 m V/A  
Output Cap. follow Intel PDDG  
330uF/9m\*2, 22uF\_0805\*6, 10uF\_0603\*6, 1uF\_0402\*11

VDD source use +5VS and PG00D source use +3VS  
Please confirm power on and down sequence,  
make sure VGATE after CPU\_CORE on.

Layout Note  
SVID routing  
1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.  
2. SVID spacing requirement is 18mils(0.475mm)  
3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).  
4. The SVID bus must be ground reference, it cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.  
5. Avoid routing under noisy circuit, e.g. switch node, Gate driver, B+, Vin, high speed signal.  
6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.



$C_n = L / ((R_{ntcnet} * R_{sum}) / (R_{ntcnet} + R_{sum})) * DCR$   
If  $C_n$  is correctly selected, when the load current has a square change, the output voltage also has a square response.

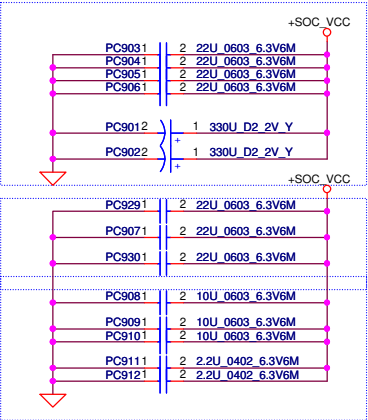


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CPU CORE/GFX CORE				Rev 1.0
Bay Trail M LA-B511P				Sheet 33 of 39
Date: Thursday, March 13, 2014				

PWR Rule  
需確認最新SPEC.  
Modify 8/6.

3 X 330u/9m(47W)  
2 X 330u/9m(37W)  
24 pcs 22uF and reserve 4 pcs  
2013/08/16

+SOC\_VCC =+CPU\_CORE



Output Cap  
(330uF\*2+22uF\*4)

Package Edge Cap  
(22uF\*3)

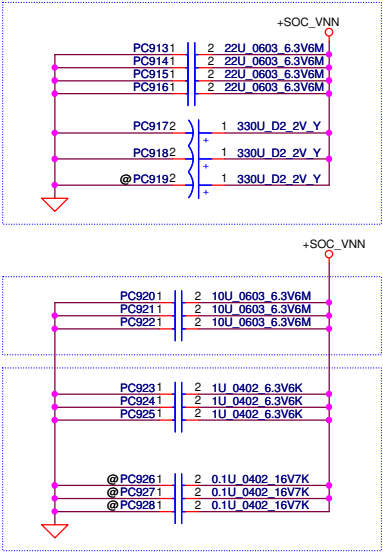
Back Side Cap  
(10uF\*1+4.7uF\*2+2.2uF\*2)

Output Cap  
(330uF\*3+22uF\*4)

Package Edge Cap  
(22uF\*3)

Back Side Cap  
(1uF\*3)

+SOC\_VNN =+VGFX\_CORE



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				Custom	Bay Trail M LA-B511P
				Date	Thursday, March 13, 2014
				Sheet	34 of 39
				Rev	1.0

## Version change list (P.I.R. List)

Page 1 of 2  
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Improve ripple voltage		30	Change PL602 from SH000000YE00 to SH0000008800	12/30	DVT
2		Improve part rating		33	Change PC901,PC902,PC917,PC918 from SGA000026800 to SGA20331E10	12/31	DVT
3	HW request	Use bead(L22) individ		29	Delete PJ501, PJ502	01/07	DVT
4		Unify VC0/VC1 setting		26	Change PR202, PR203, PR216	01/08	DVT
5		Raise part rating		32	Change PR814, PR832 size from 0402 to 0603	01/10	DVT
6		Prevent burn issue		27	Change PQ303, PQ304 from A04466L to A04406AL	01/10	DVT
7	Customer request			26	Change PR211 from 100 to 0	01/29	PVT
8		VC 0/1 controlled by sw method		28	Pop PC426	01/29	PVT
9		Meet EC request		32	Change +1.8VALW for VGATE pull high	02/18	PVT
10							
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				Date	Thursday, March 13, 2014
				Sheet	35 of 39
				Rev	1.0



## Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.08		12/17	HW	SLP_S3# leak voltage	Change Q21 direction	0.2
2	P.09		12/17	HW	GPIO_S0_SC_56 pull down no vedio. Touch screen and touch pad SMBus net fail  NO support CPU Thermal sensor	Pop R53, unpop R55 Change Q2.1 to SOC_I2C5_CLK Change Q3.1 to SOC_I2C2_CLK  Unpop U28	0.2
3	P.14		1/6	HW	U9 DP to LVDS chip old symbol	Link CIS for SA00007A300	0.2
4	P.18		1/6	HW	U14 Lid switch old symbol	Link CIS for SA000079D00	0.2
5	P.19		1/6	HW ESD	Vendor request to meet Acer spec  ESD test Fail	Change R188,R192 from 47ohm to 60.4ohm  Add C277,C278,L19,L20 for RING2 & SLEEVE Change D9 pin2.3 name to RING2_L & SLEEVE_L	0.2
6	P.6,8,11,15, 16,17,19,22		1/6	HW	0 ohm R-short	R13,R71,R72,R118,R119,R120,R121,R122, R123,R124,R125,R34,R36,R200,R254,R255, R172,R187,R193,R167,R168,R169,R170, R187,R193,R107,R108,R212	0.2
7	P.17		1/6	HW	Change LAN power	Unpop U19,C188 Pop R160,R200 change R200.2 from LAN_PWR_EN to LAN_GPO Change C204,C205 from 12pF to 10pF	0.2
8	P.22		1/6	HW	Add EC GPIO Board ID	Add LAN_GPO for U22.pin106 Change R211 to 12K	0.2
9	P.15		1/6	ESD		Add D13	0.2
10	P.21		1/6	HW	Change USB HUB to GL850S	Delete U18,R152~R157,C182~C187,Y3 Add U29,R259~R263,C279~C287,Y5	0.2
11	P.19		1/6	HW	BOM	Change C215,C273 from SE107105ML0 to SE080105K80.2	0.2
12	P.8		1/6	HW		Change R34.2 from TS_INT#_CPU to SOC_TS_INT# Change R36.2 from TP_INT#_CPU to SOC_TP_INT#	0.2
13	P.13		1/7	EMI		Add L21,L22 for EMI Change net name to +1.35V_L C91~C102,R77,R75,(JDIMM1 pin75,76,81,82,87,88, 93,94,99,100,105,106,111,112,117,118,123,124)	0.2
14	P.23		1/7	HW		Add U30,C288,C289,R264 for +3V_TP Change JTP1.8,R233.2,R225.2,R227.2 to +3V_TP	0.2

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				Bay Trail M LA-B511P	1.0
				Date: Thursday, March 13, 2014	Sheet 37 of 39

## Version Change List (P. I. R. List)

Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
15	P.24		01/07	HW	BOM	Change U24,U26 to SA00006FD00	0.2
16	P.9,23		01/08	HW	BOM	Delete TP@ BOM structure ==> C255,Q11,R223,R225,R227,R230,R63,R64,Q3	0.2
17	P.8,15,17 19,22		01/08	HW	BOM	R-short==>R34,R36,R200,R254,R255,R172,R187, R193,R167,R168,R169,R170,R187,R193,R107,R108, R212,R150,R151,R248,R249	0.2
18	P.23  P.08		01/08	HW	BOM	Pop U30,C288,C289 Unpop R264 Pop U30,C288,C289 Unpop R264	0.2
19	P.23 P.22		01/08	HW		Change U30.3 from SYSON to TP_PWR_EN Add U22.98 TP_PWR_EN	0.2
20	P.21		01/08	ME		JUSB2 Link CIS symbol ==> ACES_51524-0140N-001	0.2
21	P.21		01/13	HW		USB2.0 port0 USB3.0 conn. USB2.0 port1 USB HUB	0.2
22	P.9,14		01/14	HW		Change RP10,RP11 to 2.2K_0804_8P4R	0.2
23	P.15		01/14	HW	BOM	ETS@ BOM structure ==> R101,R102,R113,R114	0.2
24	P.21		01/16	HW	BOM	BOM structure==>Add U16,R257 to TPM@	0.2
25	P.09		02/18	HW	BOM	For +1.8VS abnormal voltage Pop R28	0.3
26	P.20		02/18	HW		For HP pop noise Change R188,R192 to 0ohm Change R187,R193 to 60.4ohm	0.3
27	P.24		02/18	HW		For TP Change R205,R206 to +3V_TP Change JTP1 pin define	0.3
28	P.23		02/18	HW		For Board ID Pop R219 Change R221 to 15K	0.3
29	P.25		02/18	HW		For +1.0 VS Pop C268, Change R242 to 1K	0.3
30	P.24		02/18	HW		unpop SW2	0.3

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				Date:	Thursday, March 13, 2014
				Sheet	38 of 39
				Rev	1.0

## Version Change List ( P. I. R. List )

Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
31	P. 20, 24		02/21	ME		JKB2, JBL1, JDMIC1 蓋綠漆. Change footprint to XXXX-S	0.3
32	P. 9, 21, 22, 23		02/21	HW		R-short R40, R96, R143, R142, R259, R198, R199, R220	0.3
32	P. 9		02/21	HW		Add JCMOS2	0.3
33	P. 24		02/21	ME		測光 Chang R231, R233 to 100 ohm Change R232, R234 to 470 ohm	0.3
34	P. 22		02/24	HW		Change USB HUB to GL850G Add U31, R265, R266, R267 Delete U29, R262	0.3
35	P. 09		02/25	HW		32.768KHz Change C17, C18 to 18pF	0.3
36	P. 17, 20, 25		02/26	HW		Change Q9, Q17, Q18 from SB00000DH00 to SB00000ZU00	0.3
37	P. 16		03/12	HW		R-short R88	1.0
38	P. 23		03/13	HW		For Board ID Change R221 from 15K to 20K	1.0
39	P. 24		03/13	HW		Change SW1 from DBG@ to @	1.0

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				Document Number	Bay Trail M LA-B511P	
Date:				Thursday, March 13, 2014	Sheet	39 of 39